pRU Address Map

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Identical modules are separated with a fixed base address offset of 0x1000. I.e. alpide_data for chip ID 0 on stave 0, has base address 0x2300_0000, while alpide_data for chip ID 1 on stave 0, has base address 0x2300_1000, and so on.

Module	Clock Domain [MHz]	Base Address	Module Range	Total address space	Num modules
global_regs	31.25	0x2000_0000	0x0 - 0xFFF	0x2000_0000 - 0x2000_0FFF	1
sysmon	31.25	0x2010_0000	0x0 - 0xFFF	0x2010_0000 - 0x2010_0FFF	1
dna	31.25	0x2020_0000	0x0 - 0xFFF	0x2020_0000 - 0x2020_0FFF	1
trigger_manager	40	0x2100_0000	0x0 - 0xFFF	0x2100_0000 - 0x2100_0FFF	1
alpide_control	40	0x2140_0000	0x0 - 0xFFF	0x2140_0000 - 0x2140_0FFF	1
offload	120	0x2200_0000	0x0 - 0xFFF	0x2200_0000 - 0x2200_1FFF	1
alpide_data	120	0x2300_0000	0x0 - 0xFFF	0x2300_0000 - 0x2306_BFFF	108

Table 1: pRU Address map

Note about PTB

For PTB, and potential other implementations on Zync FPGAs, the base addresses has a prefix of 0x05, i.e. the address is a total of 5 bytes. This prefix should be added in the embedded software, and thus ignored by all host software. PTB does NOT incorporate SYSMON and DNA.

Module	Clock Domain [MHz]	Base Address	Module Range	Total address space	Num modules
ptb_regs	40	0x2180_0000	0x0 - 0xFFF	0x2180_0000 - 0x2180_0FFF	1
power_control	100	0x2400_0000	0x0 - 0xFFF	0x2400_0000 - 0x2400_0FFF	1

Table 2: PTB Specific Modules

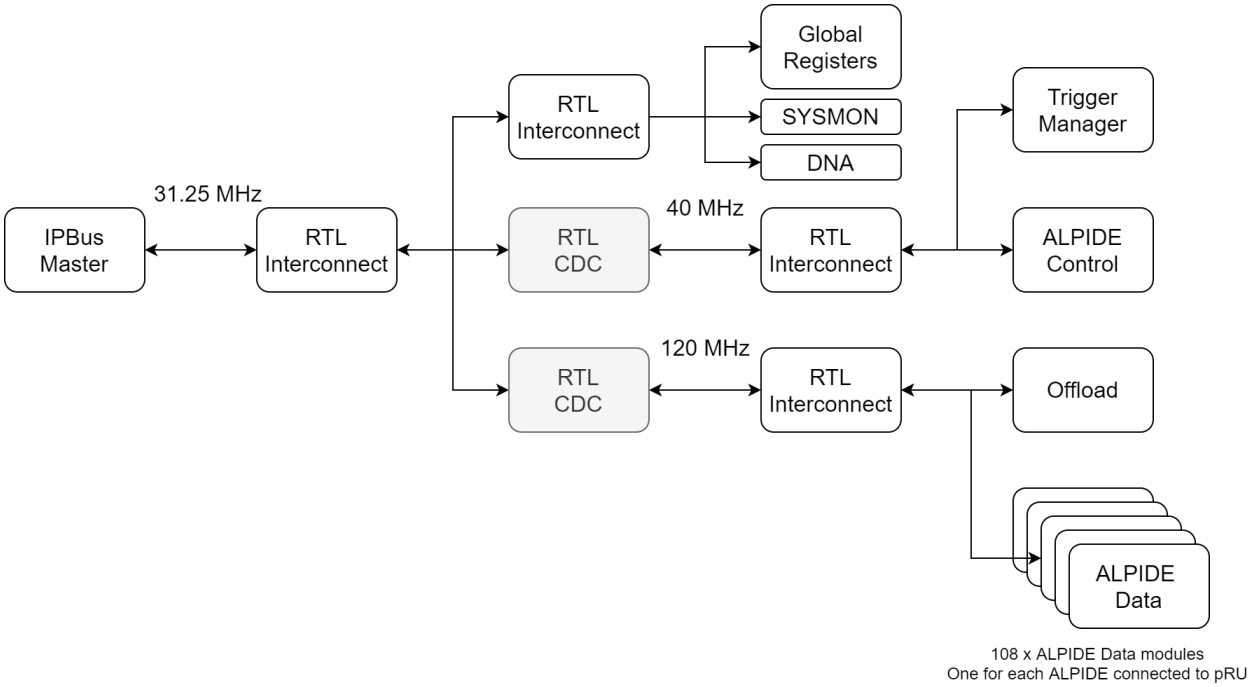

Figure 1: Bus tree