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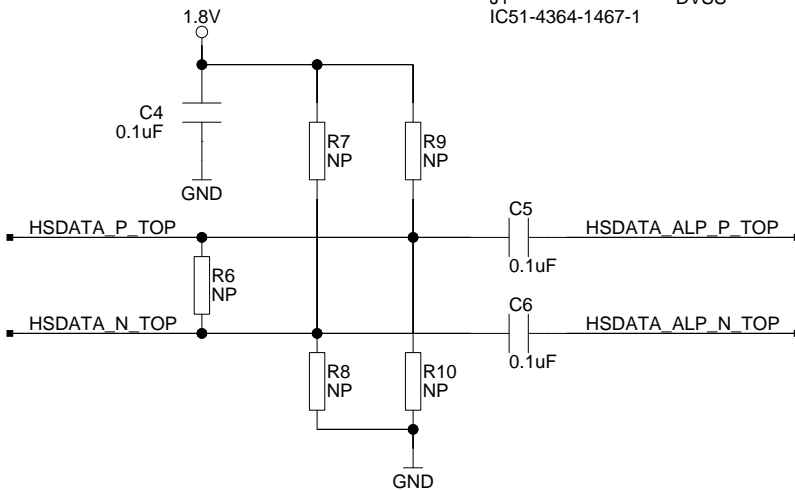
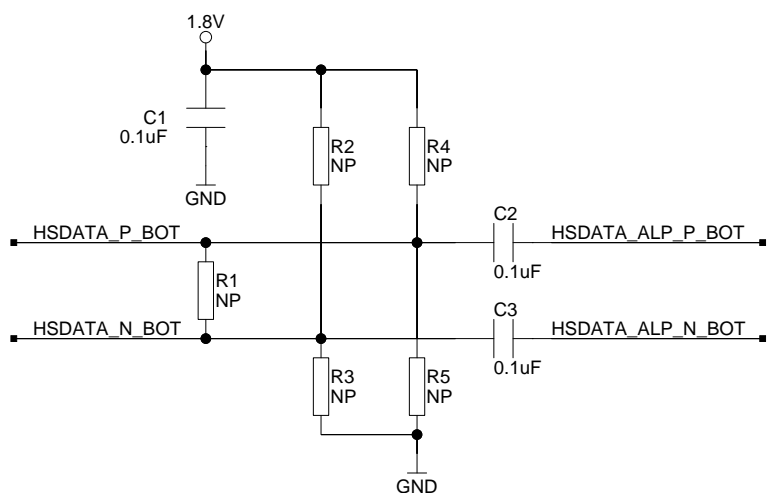
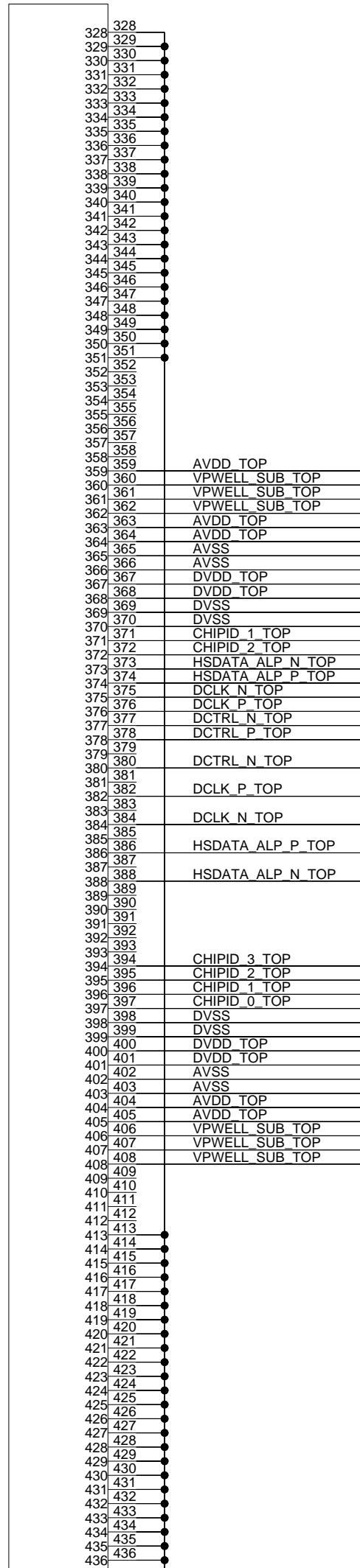
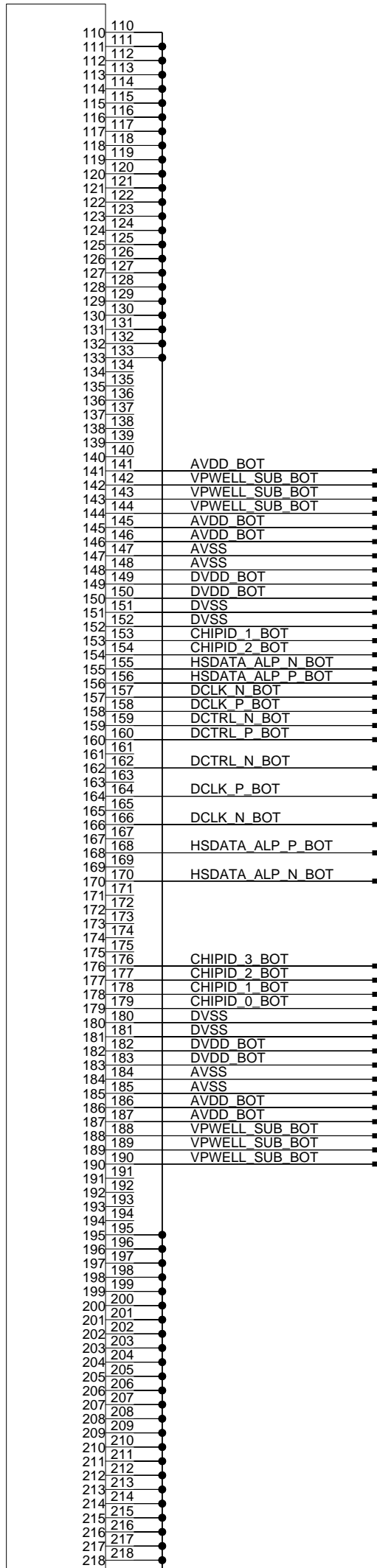
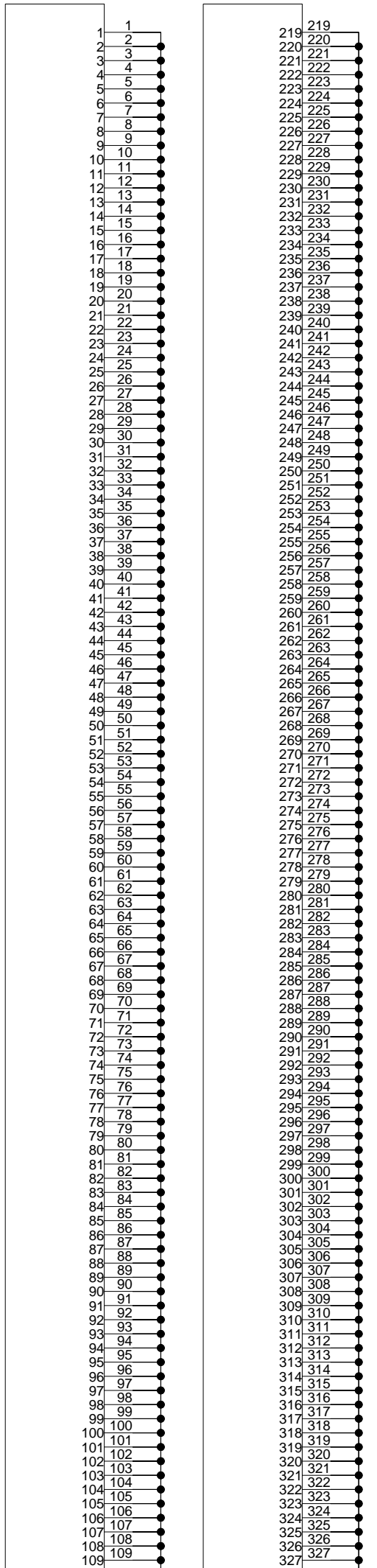
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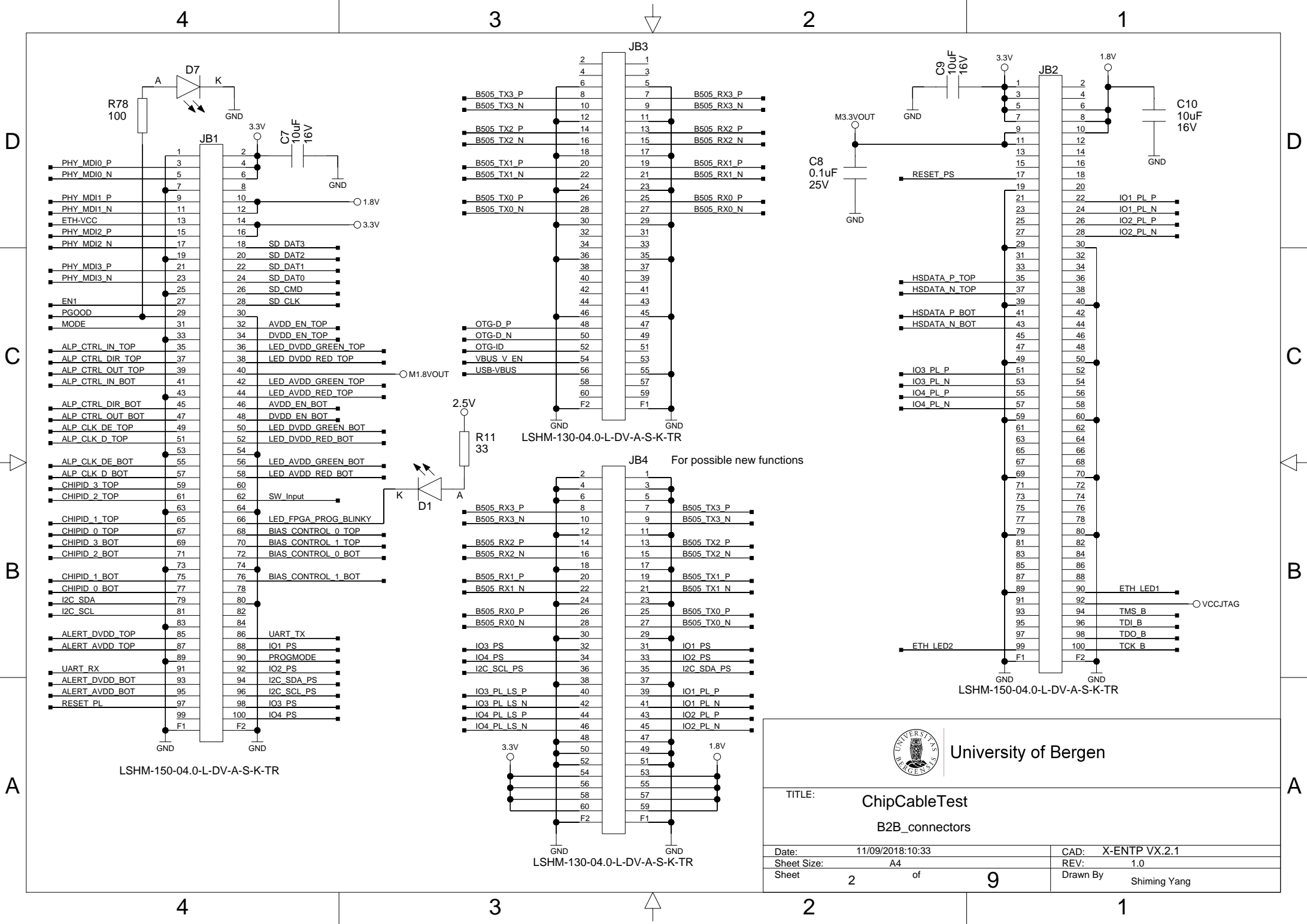




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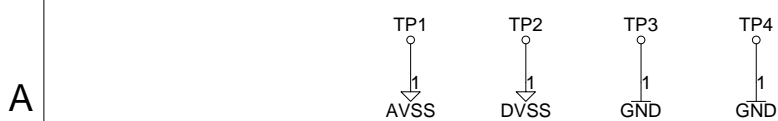
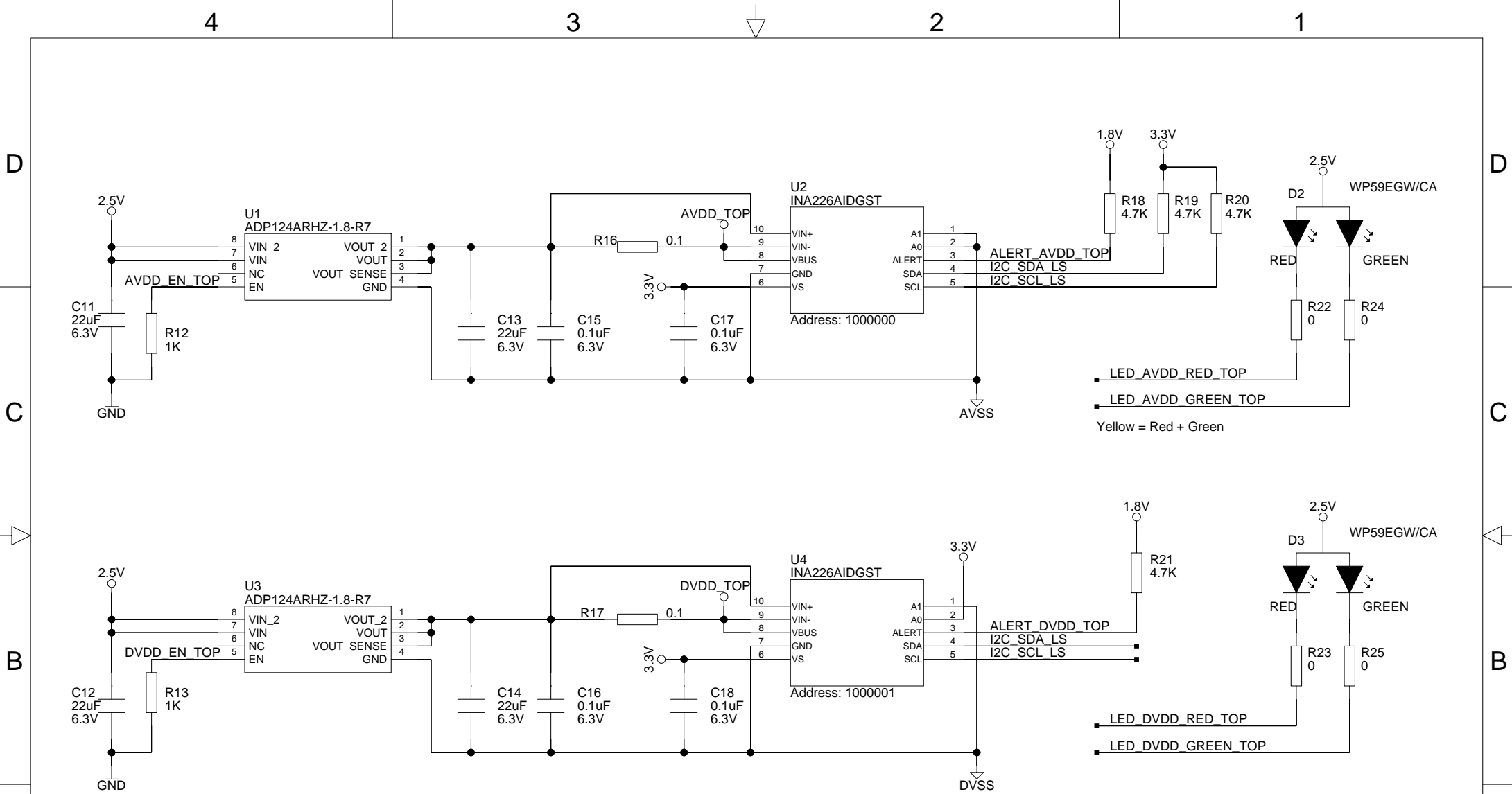
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YamaichiSocket

Date:	06/09/2018:11:18	CAD:	X-ENTP VX.2.1
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Sheet	1 of 9	Drawn By	Shiming Yang



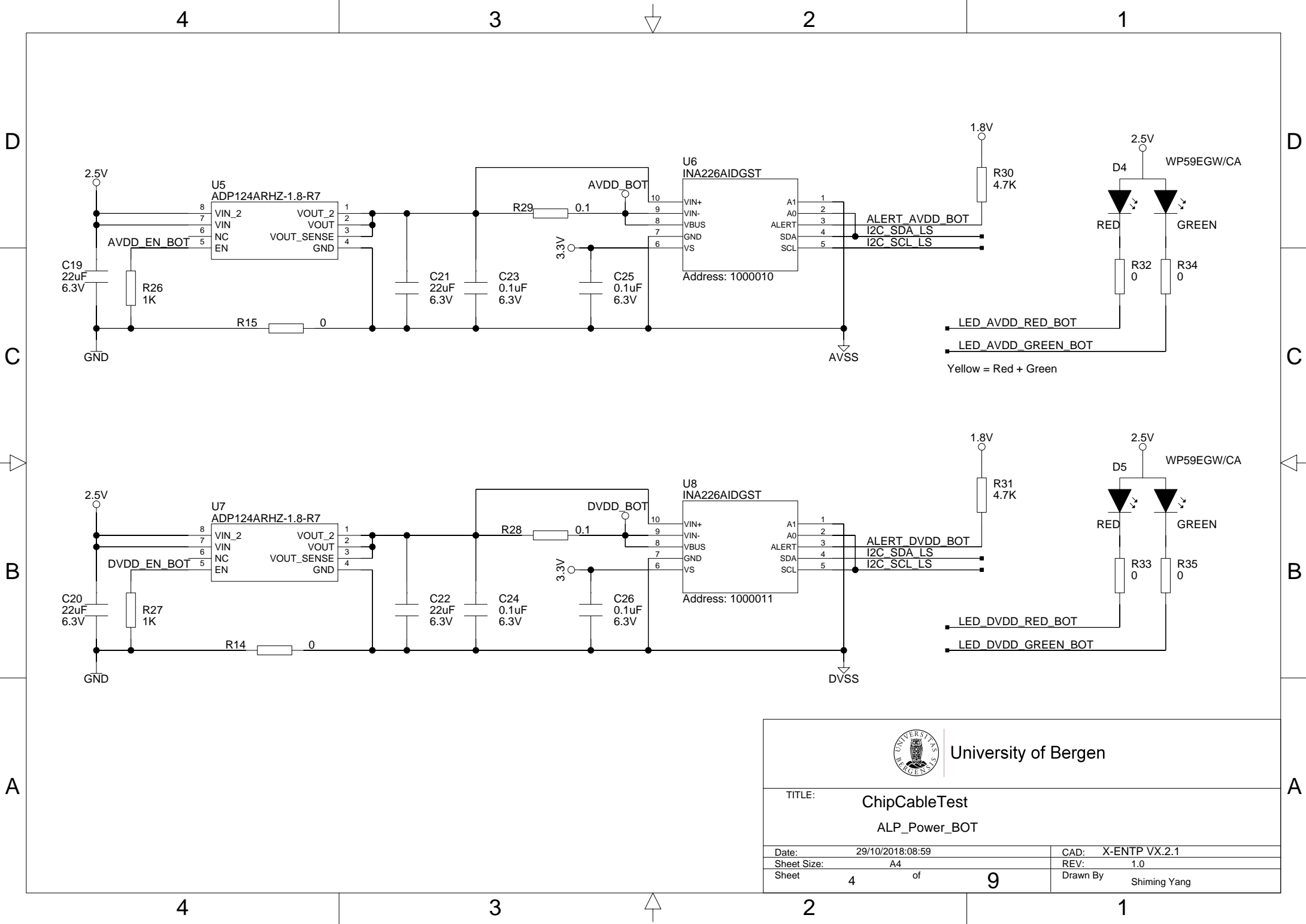
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TITLE: ChipCableTest		
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Sheet 2 of 9	Drawn By Shiming Yang	



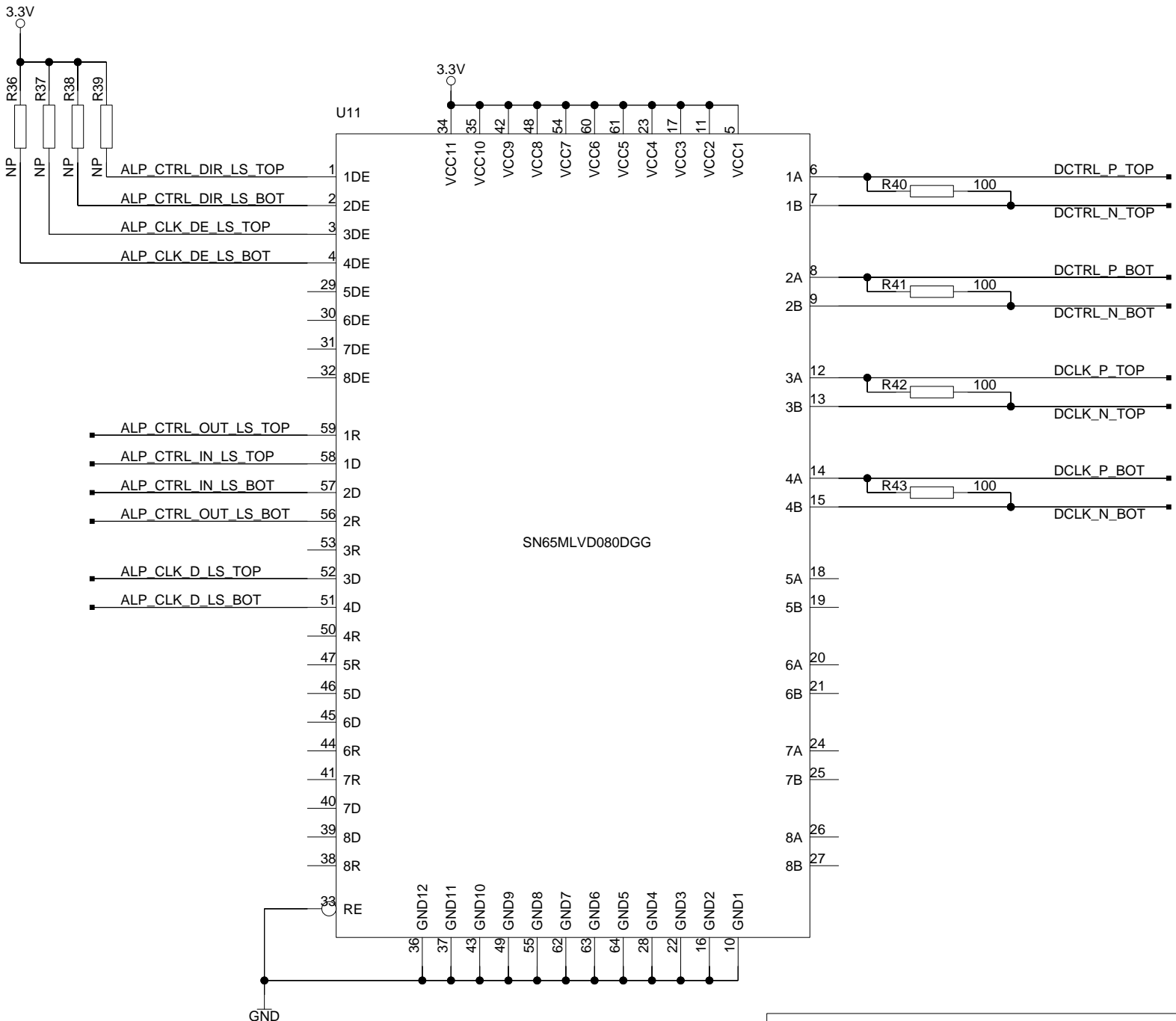
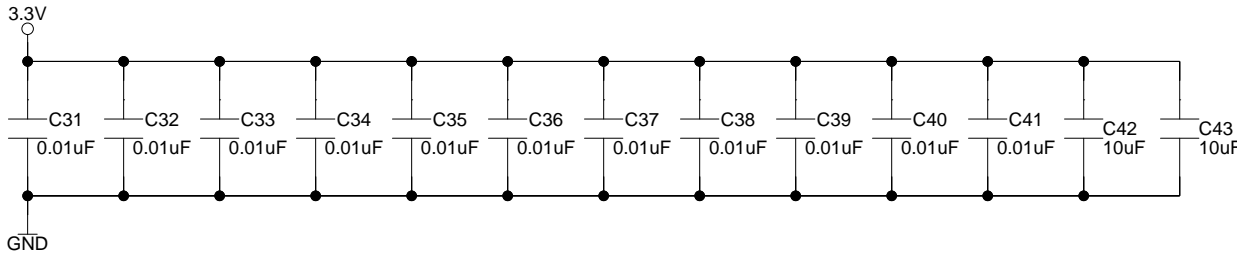
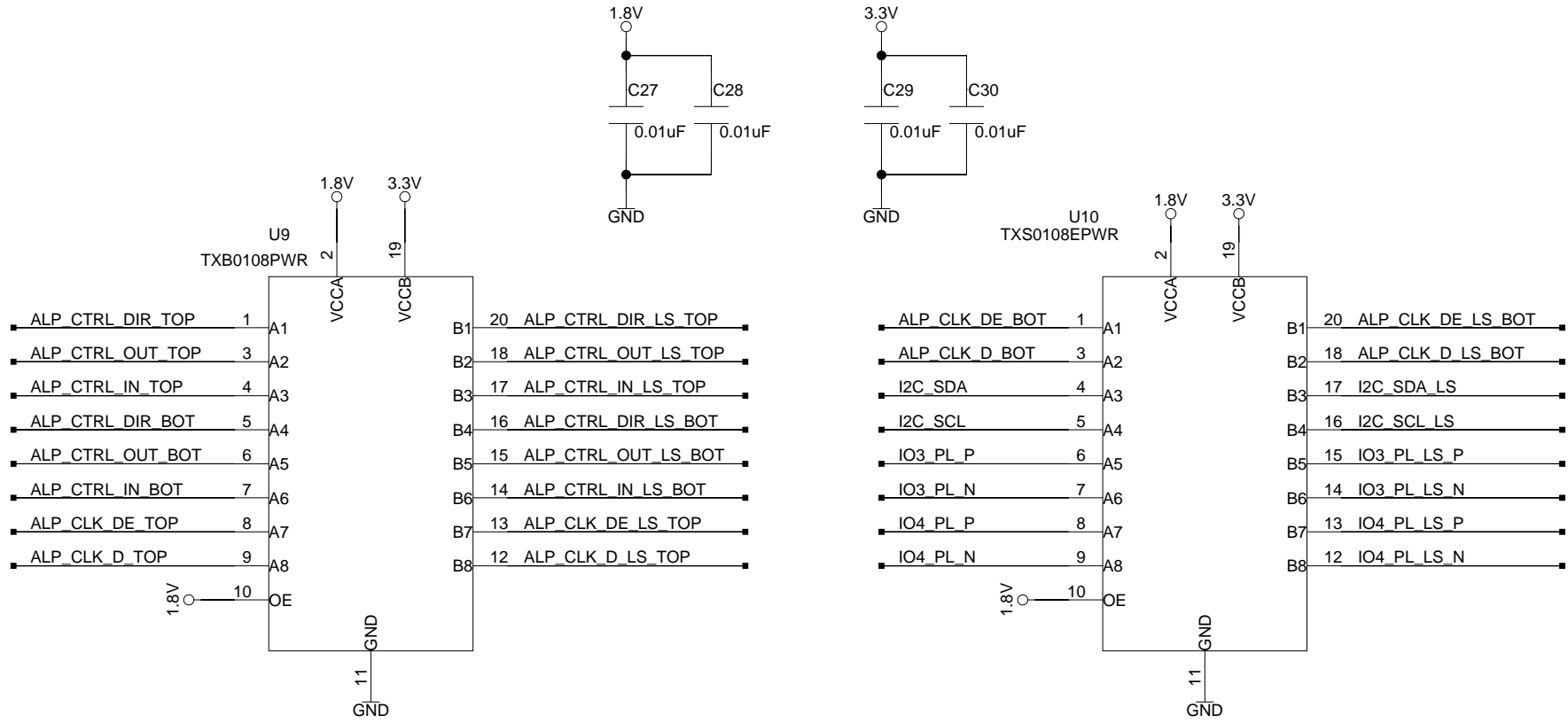
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Date: 29/10/2018:08:59	CAD: X-ENTP VX.2.1
Sheet Size: A4	REV: 1.0
Sheet 3 of 9	Drawn By Shiming Yang



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Date:	29/10/2018:08:59	CAD:	X-ENTP VX.2.1
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TITLE: **ChipCableTest**
ALP_Control

Date: 24/10/2018:13:24	CAD: X-ENTP VX.2.1
Sheet Size: A3	REV: 1.0
Sheet 5 of 9	Drawn By: Shiming Yang

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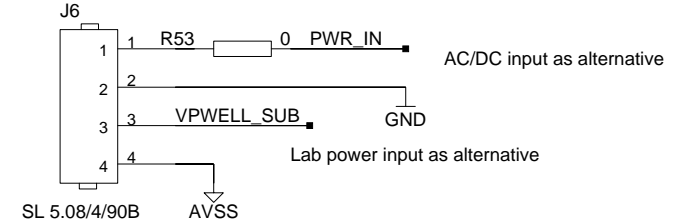
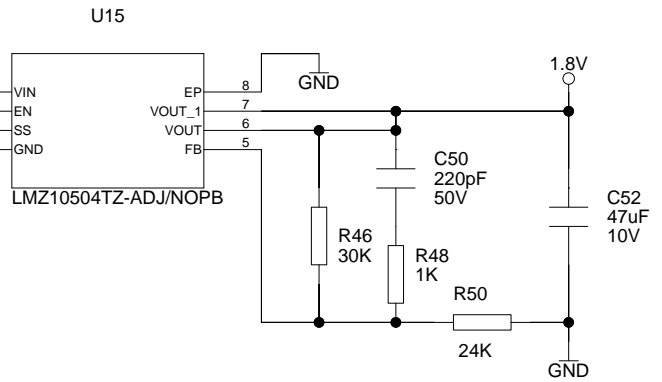
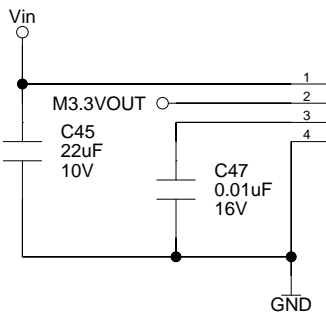
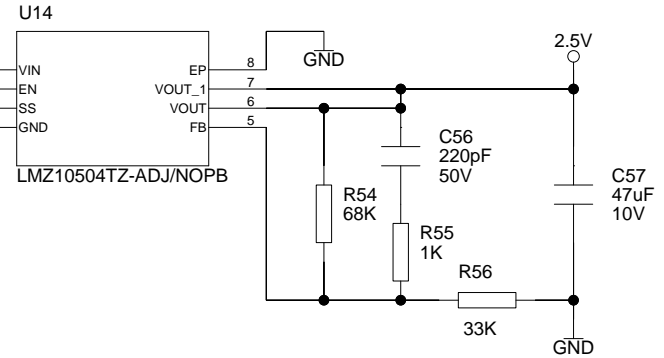
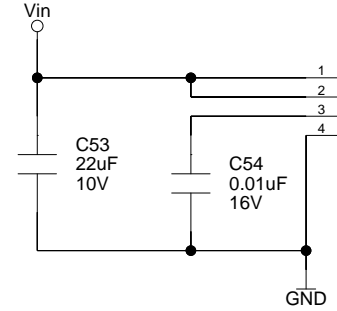
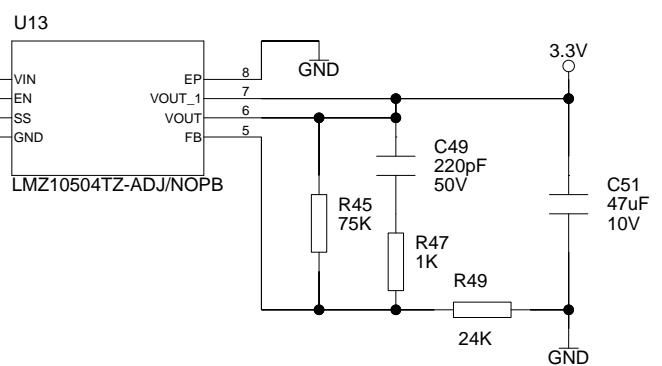
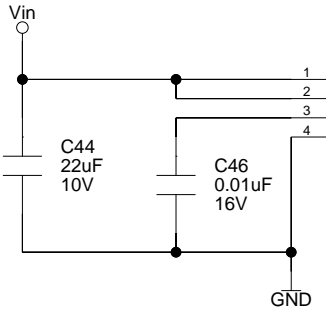
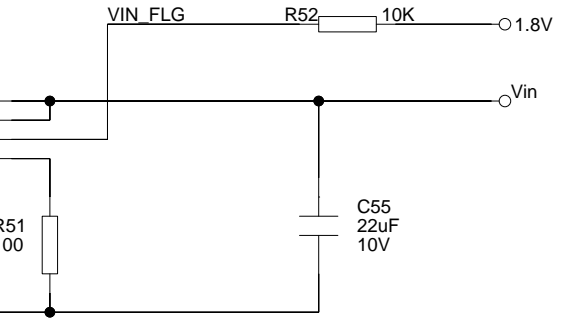
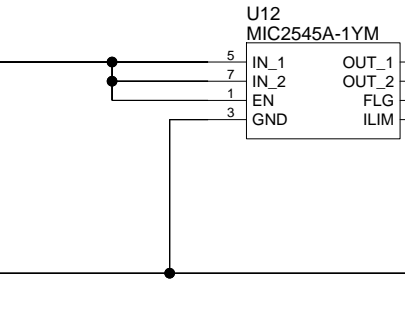
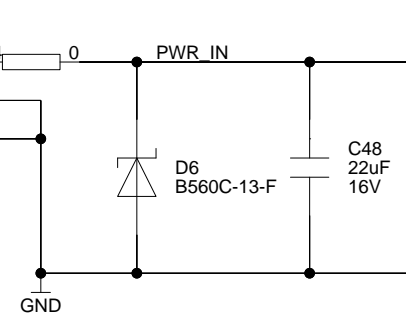
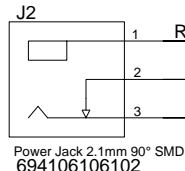
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TITLE: ChipCableTest
Power

Date: 05/10/2018:11:18
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Sheet 6 of 9

CAD: X-ENTP VX.2.1
REV: 1.0
Drawn By: Shiming Yang

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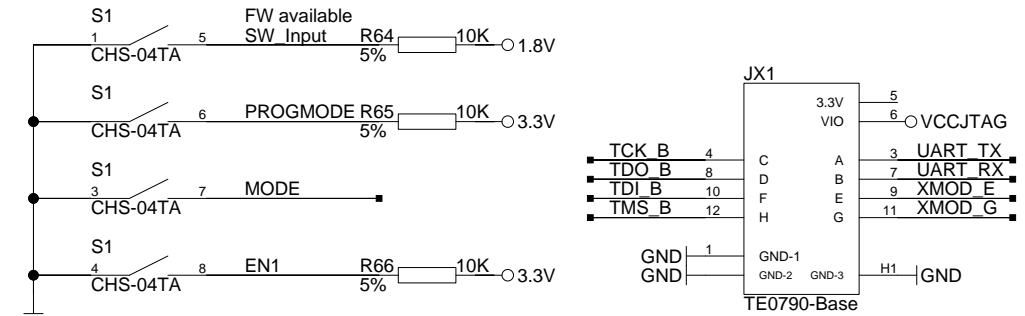
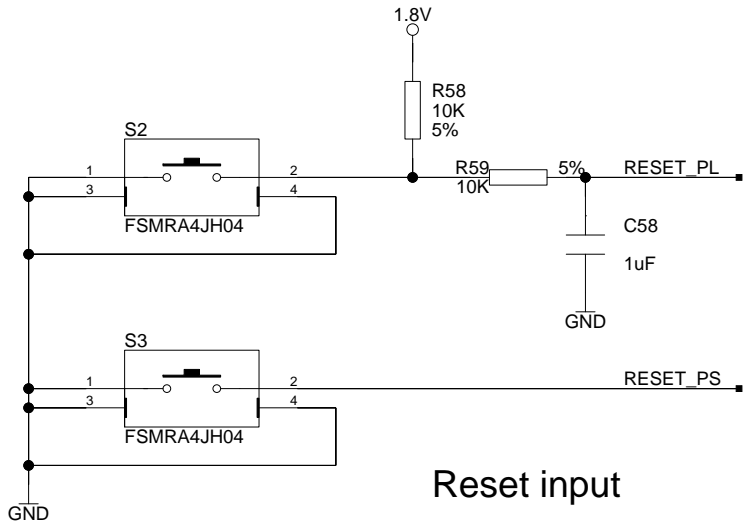
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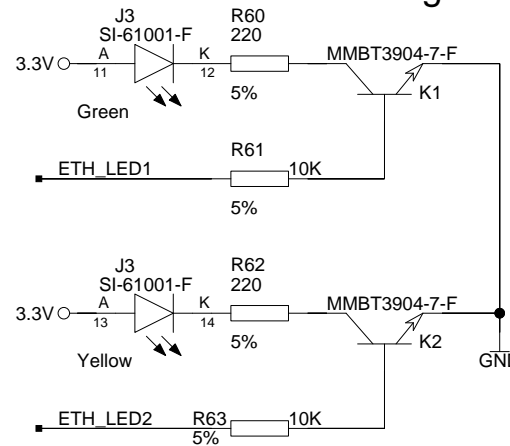
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XMOD-FT2232H header: JTAG and UART

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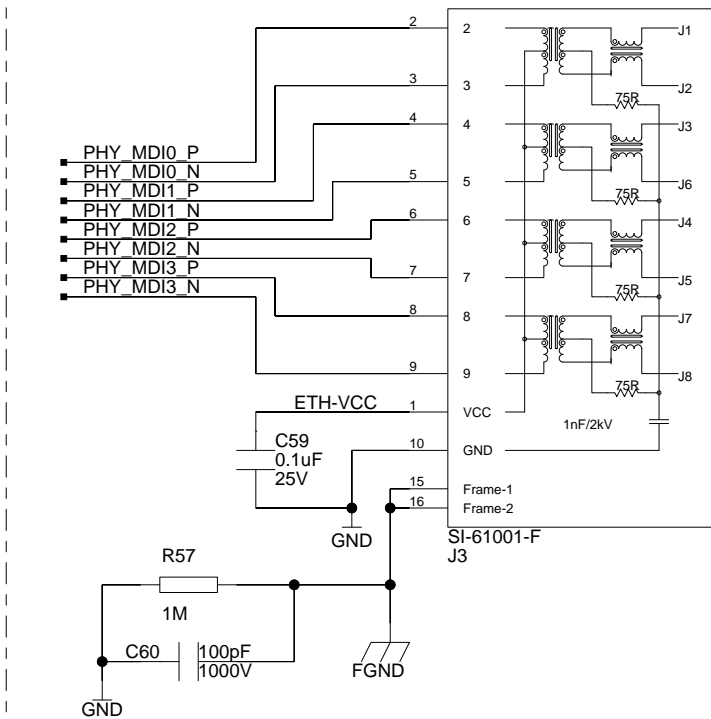
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Gigabit Ethernet



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TITLE: **ChipCableTest**
Interface1

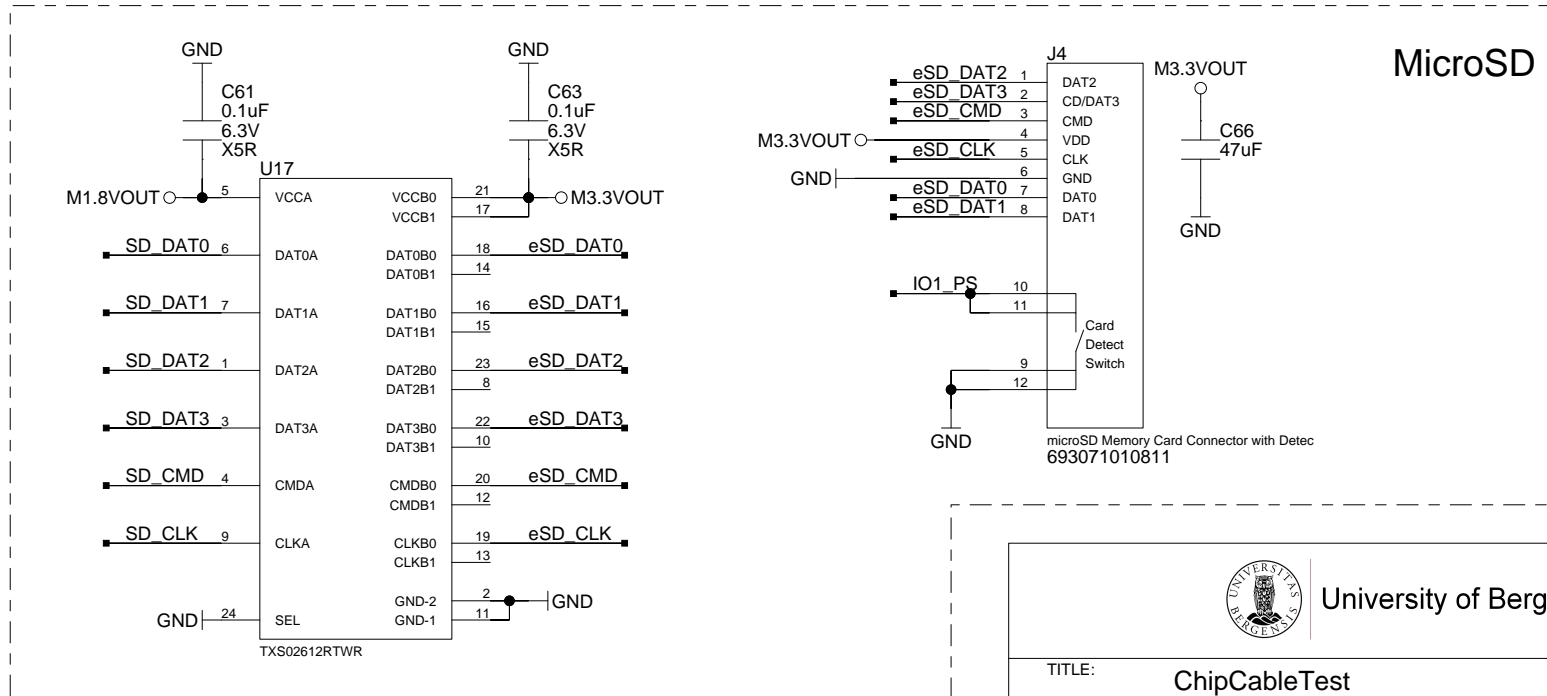
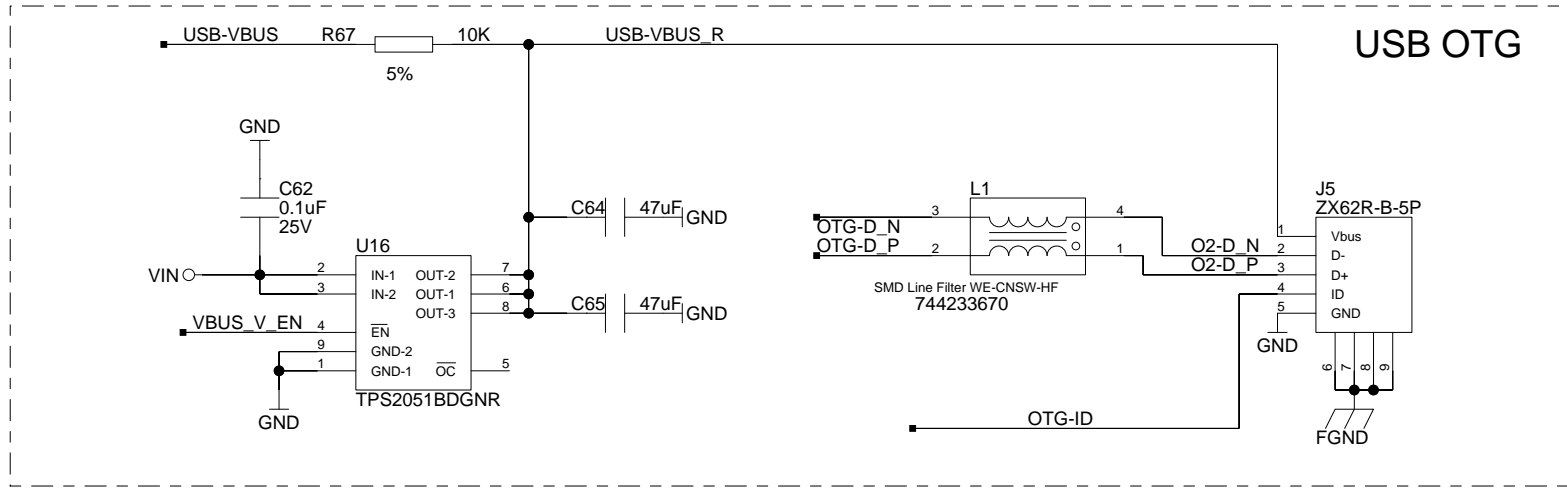
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Sheet	7 of 9	Drawn By	Shiming Yang

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TITLE: **ChipCableTest**
Interface2

Date:	09/08/2018:13:33	CAD:	X-ENTP VX.2.1
Sheet Size:	A4	REV:	1.0
Sheet	8 of 9	Drawn By	Shiming Yang

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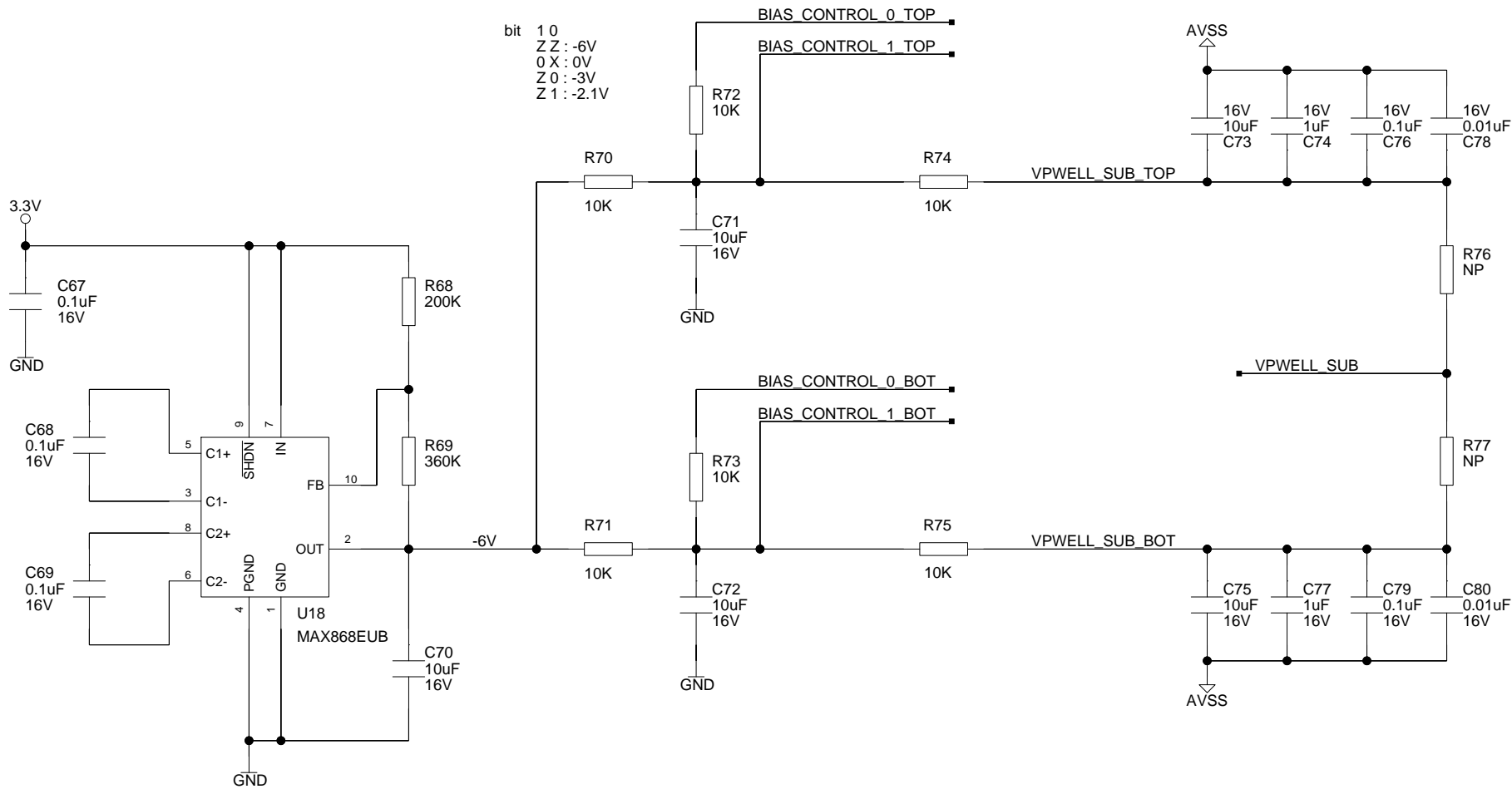
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bit 1 0
 ZZ : -6V
 0 X : 0V
 Z 0 : -3V
 Z 1 : -2.1V



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TITLE: ChipCableTest
 VPWELL

Date: 11/09/2018:11:33
 Sheet Size: A4
 Sheet 9 of 9

CAD: X-ENTP VX.2.1
 REV: 1.0
 Drawn By Shiming Yang