

## alpide\_data

Version: 1.1

Sunday 8<sup>th</sup> November, 2020 20:42

Control and status of ALPIDE data readout.

## 1 Register List

#	Name	Mode	Address	Type	Length	Reset
0	run_settings	RW	0x00000000	FIELDS	3	0x0
1	module_ids	RO	0x00000001	FIELDS	8	0x0
2	run_status	RO	0x00000002	FIELDS	9	0x0
3	reset_counters	PULSE	0x00000003	SL	1	0x0
4	num_prbs_error	RO	0x00000004	DEFAULT	32	0x0
5	num_decode_error_0	RO	0x00000005	DEFAULT	32	0x0
6	num_decode_error_1	RO	0x00000006	DEFAULT	32	0x0
7	num_protocol_error	RO	0x00000007	DEFAULT	32	0x0
8	num_frame_error	RO	0x00000008	DEFAULT	32	0x0
9	num_frames	RO	0x00000009	DEFAULT	32	0x0
10	num_empty_frames	RO	0x0000000A	DEFAULT	32	0x0
11	num_busy	RO	0x0000000B	DEFAULT	32	0x0
12	num_busy_violation	RO	0x0000000C	DEFAULT	32	0x0
13	num_flushed_incomplete	RO	0x0000000D	DEFAULT	32	0x0
14	num_strobe_extended	RO	0x0000000E	DEFAULT	32	0x0
15	num_busy_transition	RO	0x0000000F	DEFAULT	32	0x0
16	num_data_overrun	RO	0x00000010	DEFAULT	32	0x0
17	num_fatal_condition	RO	0x00000011	DEFAULT	32	0x0
18	num_buffer_overflow	RO	0x00000012	DEFAULT	32	0x0
19	num_frames_dropped	RO	0x00000013	DEFAULT	32	0x0
20	num_fake_frames	RO	0x00000014	DEFAULT	32	0x0

## 2 Registers

Register 2.1: RUN\_SETTINGS - RW (0x00000000)  
Run settings register.

31	unused	3	prbs_test	test_mode	run
-			2	1	0
-			0	0	0

Reset

- run** De-asserts DPA channel reset. Enables 8B10B decoder after 100 clock cycles.
- test\_mode** Enable test mode functionality. Disables the data flow blocks of the module. To be asserted together with the run bit before a PRBS test.
- prbs\_test** Enable PRBS-7 test mode functionality - counting number of PRBS-7 errors. test\_mode bit must be asserted PRIOR to asserting this bit to avoid counting wrong.

Register 2.2: MODULE\_IDS - RO (0x00000001)  
The chip and stave ID associated with the module.

31	unused	8	chip_id	stave_id
-			7	3
-			4	0
-			0x0	0x0

Reset

- stave\_id** Stave ID - used for tagging pRU data words.
- chip\_id** Chip ID - used for tagging pRU data words.

Register 2.3: RUN\_STATUS - RO (0x00000002)  
Run status register.

31	unused	9	buffer_status	data_formatter_status	data_aligned	enable_alignment	fifo_empty	loss_of_signal	
-			8	5	4	3	2	1	0
-			6	4	3	2	1	0	
-			0x0	0x0	0	0	0	0	

Reset

- loss\_of\_signal** DPA logic lost signal.
- fifo\_empty** CDC FIFO is empty.
- enable\_alignment** Data processing is started.
- data\_aligned** Data is aligned and 8B10B decoding started.
- data\_formatter\_status** 0 = idle, 1 = processing frame, 2 = waiting for free space (buffer full).
- buffer\_status** 0 = empty, 1 = almost empty, 2 = prog empty, 3 = some data, 4 = prog full, 5 = full.

Register 2.4: RESET\_COUNTERS - PULSE FOR 1 CYCLES (0x00000003)  
Resets all counters in module.

31	1	0	
-			0
			Reset

Register 2.5: NUM\_PRBS\_ERROR - RO (0x00000004)  
Number of PRBS-7 errors in PRBS test mode.

31	0	
0x0		Reset

Register 2.6: NUM\_DECODE\_ERROR\_0 - RO (0x00000005)  
Number of 8B10B decode errors observed - bits 31:0.

31	0	
0x0		Reset

Register 2.7: NUM\_DECODE\_ERROR\_1 - RO (0x00000006)  
Number of 8B10B decode errors observed - bits 63:32.

31	0	
0x0		Reset

Register 2.8: NUM\_PROTOCOL\_ERROR - RO (0x00000007)  
Number of protocol errors observed. Protocol errors are all decode errors observed during processing of an frame, but also all other protocol errors e.g. a double busy on assertion.

31	0	
0x0		Reset

Register 2.9: NUM\_FRAME\_ERROR - RO (0x00000008)  
Number of frames with errors observed. These errors are fatal, i.e. they cause the processing of the frame to be aborted and an immediate generation of the pRU trailer word.

31	0	
0x0		Reset

Register 2.10: NUM\_FRAMES - RO (0x00000009)  
Number of ALPIDE frames registered. Is incremented when the protocol checker is asserting that processing of a complete frame is done. However, this may include frames with fatal errors.

31	0	
0x0		Reset

Register 2.11: NUM\_EMPTY\_FRAMES - RO (0x0000000A)  
Number of empty ALPIDE frames registered.

31	0	
0x0		Reset

Register 2.12: NUM\_BUSY - RO (0x0000000B)  
Number of busys observed.

31	0
0x0	

Reset

Register 2.13: NUM\_BUSY\_VIOLATION - RO (0x0000000C)  
Number of busy violation events indicated by the ALPIDE chip.

31	0
0x0	

Reset

Register 2.14: NUM\_FLUSHED\_INCOMPLETE - RO (0x0000000D)  
Number of flushed incomplete events indicated by the ALPIDE chip.

31	0
0x0	

Reset

Register 2.15: NUM\_STROBE\_EXTENDED - RO (0x0000000E)  
Number of strobe extended framing windows indicated by the ALPIDE chip.

31	0
0x0	

Reset

Register 2.16: NUM\_BUSY\_TRANSITION - RO (0x0000000F)  
Number of busy transitions indicated by the ALPIDE chip.

31	0
0x0	

Reset

Register 2.17: NUM\_DATA\_OVERRUN - RO (0x00000010)  
Number of data overruns indicated by the ALPIDE chip.

31	0
0x0	

Reset

Register 2.18: NUM\_FATAL\_CONDITION - RO (0x00000011)  
Number of fatal conditions indicated by the ALPIDE chip.

31	0
0x0	

Reset

Register 2.19: NUM\_BUFFER\_OVERFLOW - RO (0x00000012)  
Number of buffer overflows observed.

31	0
0x0	

Reset

Register 2.20: NUM\_FRAMES\_DROPPED - RO (0x00000013)  
Number of full frames dropped because over buffer overflow.

31	0
0x0	

Reset

Register 2.21: NUM\_FAKE\_FRAMES - RO (0x00000014)  
Number of ALPIDE frames rejected because of mismatch of chip ID. Will only be counted if  
global\_regs/check\_id register is set.

31	0
0x0	
Reset	