Readout Electronics Status

Ola S Grøttvik

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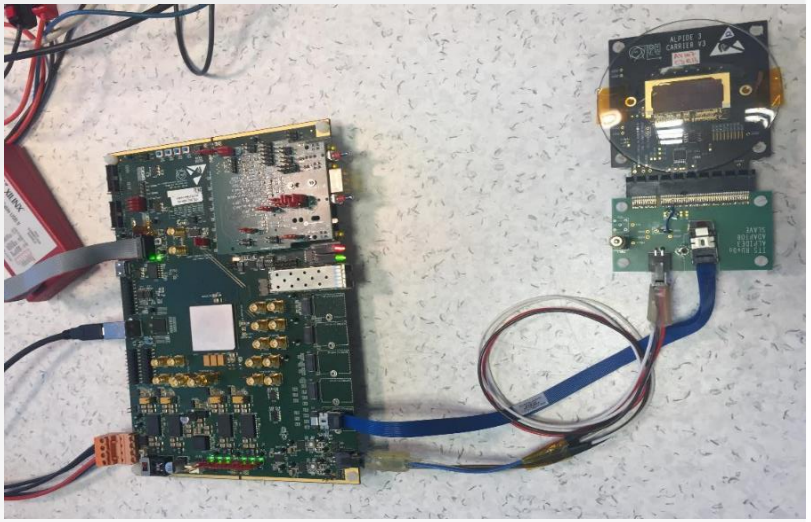
Previous work

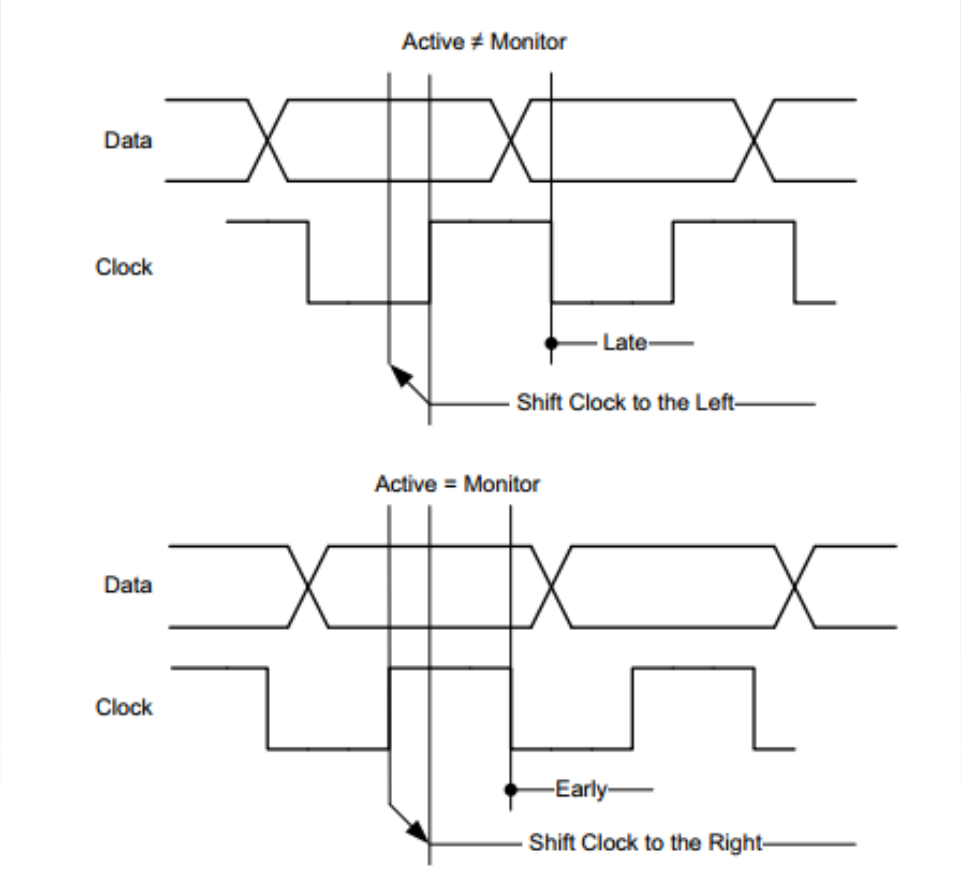
- Combined efforts with ITS
  - Use of same readout unit
  - Xilinx Kintex 7
- Focus on employing regular I/O pins for data sampling
  - Will increase the amount of ALPIDE channels connected to RU
  - Developed new FPGA firmware that successfully obtained reliable data with 2m Firefly cables (very low BER)
- Complete simulation testbench for entire readout system
- Software developed for extensive testing



Board and FPGA-Update

- New readout board (Xilinx VCU118 evaluation kit)
  - Has multiple features that enable test of various schemes
  - Current development largely independent of ITS
- New Xilinx Virtex Ultrascale+ FPGA
  - More resources for buffering and various other tasks
- New IO Architecture
  - New theoretically improved sampling method
  - More complex
    - Required time consuming firmware update
- Produced adapter PCB for connection to various ALPIDE-boards
- Use of softcore processor for control communication
  - Protocol for reducing communication errors
  - Both USB UART and Ethernet

New sampling method



New sampling method

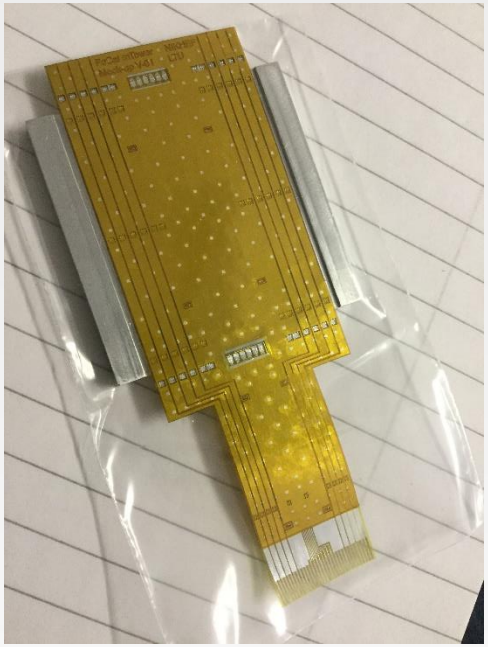
- Reduced resource usage
- Reduced calibration time
- Continuous phase tracking
  - Will theoretically cancel out ALPIDE jitter (needs testing)
- Cutting-edge -> implementation bugs (still in Xilinx beta)
- Very time-consuming to implement and do changes in architecture until Xilinx fixes wizard

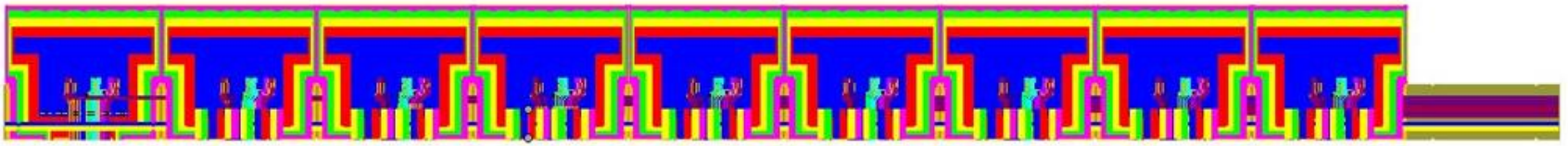
News (April 2018):

- Developed scalable firmware that greatly reduce implementation/alteration time
- Test Results:
  - Extremely low BER
  - A few issues in ~0.1% of runs -> some troubleshooting required

COOP with Utrecht/Kharkiv

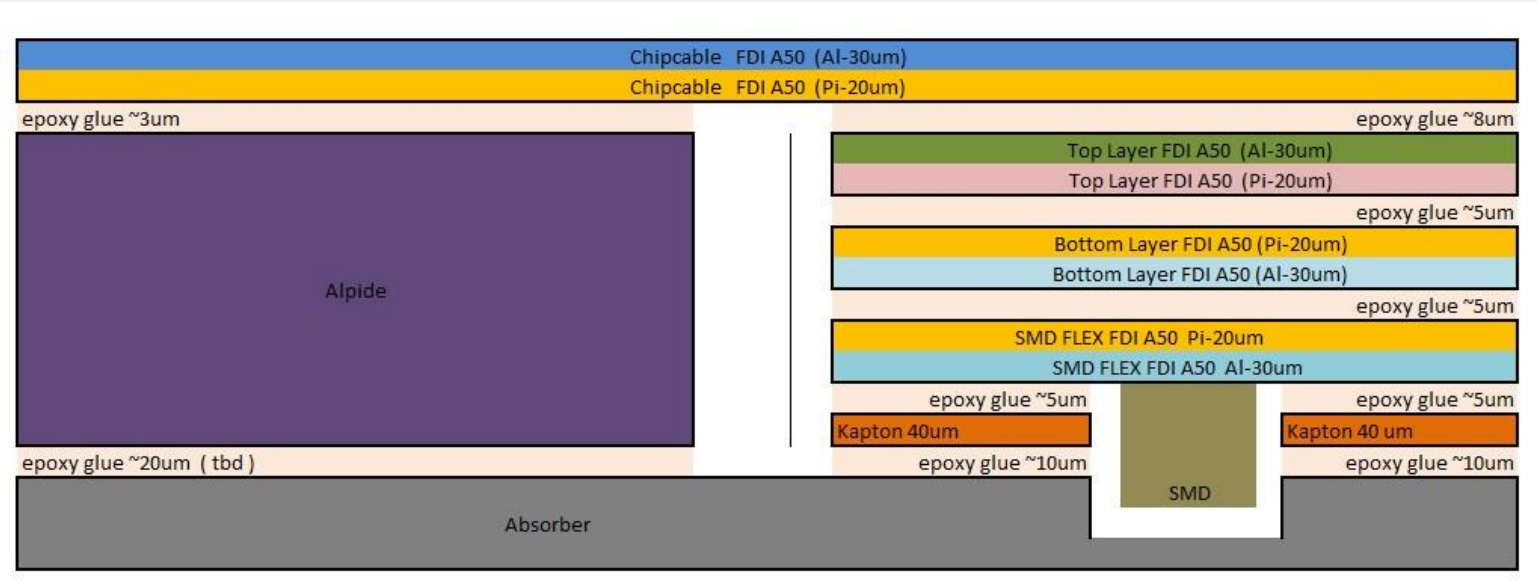
- 2-chip aluminium carrier
  - Routing of chip ID to build 8-chip modules
  - Ready for testing
    - Currently located in Utrecht
- 9-chip slab for pCT
  - Waiting for impedance test results
    - Currently tests done in Utrecht
    - Possible tests in Bergen
- Utrecht: PCBs for connection to Bergen RU
- Bergen ready for testing functionality of both systems





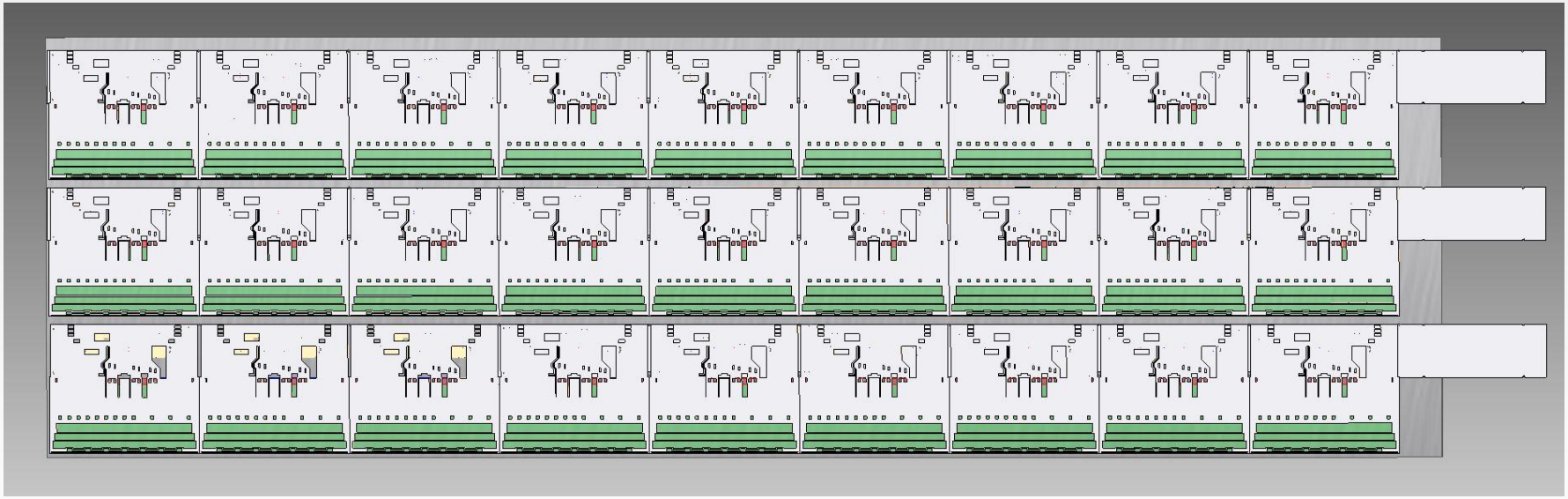
COOP with Utrecth/Kharkiv

Cross section of detector layer – 9-chip slab



COOP with Utrecth/Kharkiv

- 3-string structure
- Detector layer base (x4 -> 36 chips)



Test systems and prototypes

- Production Test Box (PTB)
  - Testing of ALPIDE's mounted to Al chip-cables in Ukraine
  - Speed up production of 9-chip strings
- mTower
  - Beam tests
- Mini Focal (Utrecht)
  - Beam tests

One RU for all systems?

- Interface 24 ALPIDE chips

- Current baseline:
  - Trenz TE820, MPSoC Module with Xilinx Zynq UltraScale+ ZU4CG-1E
  - Affordable
    - Multiple systems can be produced
  - Reuse of firmware/software from VCU118 development

Challenges / Opportunities

- Significantly reduced on-chip RAM for buffering
  - Restricts on-chip event building
  - Forces a new data format and firmware-update
- Only 1 GB on-board RAM for buffering
  - May require high-bandwidth offload
    - In communication with two individual proprietary hardware TCP/IP IP vendors
    - Alternative: Software stack TCP/IP
    - Alternative: Open-hardware UDP IP?
- For PTB:
  - Requires software-wrapper to CERN APIDE test software
  - Requires ALPIDE testing expertise
- For beam tests:
  - Requires software suite

Dataformat

- Dataformat specification document «complete» and available
  - Current specification includes possibilities for addition of more metrics, versioning, etc…
- FPGA firmware under development
- Ready for software development
  - Event building
  - Protocol checking
  - Auto-creation of ROOT-files, etc…

1.1 General format [127:0]

Name	WORD_TYPE	RU	STAVE	CHIPID	CONTENT
Length	2	6	4	4	112
Bits	127:126	125:120	119:116	115:112	111:0

WORD_TYPE Determines the type of pRU word.

- **0x0** DATA_WORD
- **0x1** TAG_HEADER_WORD
- **0x2** TAG_TRAILER_WORD
- **0x3** TAG_EMPTY_WORD

RU Identification of which specific readout unit the data originated from.

STAVE Identification of which specific stave the data originated from.

CHIPID Identification of which specific ALPIDE chip the data originated from.

CONTENT Either collection of ALPIDE data or pRU tag data.

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