IB Flexible Printed Circuit

Antonello Di Mauro - CERN

ALICE ITS Upgrade

Stave Production Readiness Review

CERN, 27 April 2017

Design Requirements

- Low material budget

The choice of the material to be used for the metal layers of the FPC is dictated by the need to minimise the material budget, thus Al has been preferred to the standard Cu (the respective radiation lengths being 8.9 cm and 1.44 cm).

- Small losses and minimum impedance for homogenous power supply along the detector modules (9 pixel sensors row) and high quality of control and readout signals

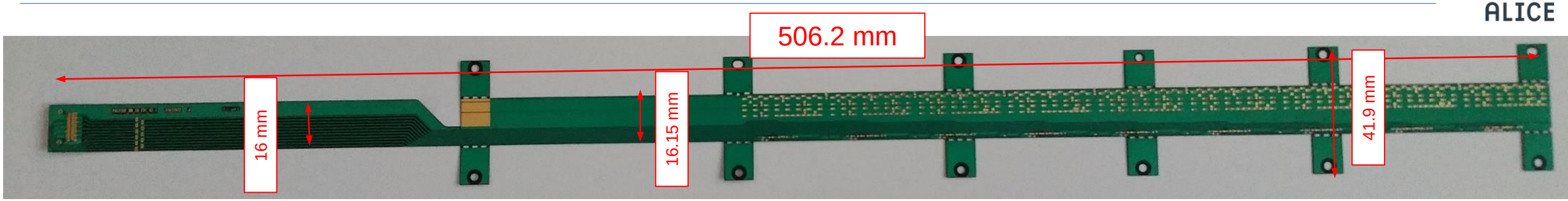
The thickness of each Al layer is 25 µm, a value which allows keeping at the desired value (< ~50 mV) voltage variations along the power supply lines; in addition, with a thickness of 75 µm for the polyimide substrate (Upilex-75S), a differential impedance of 100 Ω in the signal lines is obtained.

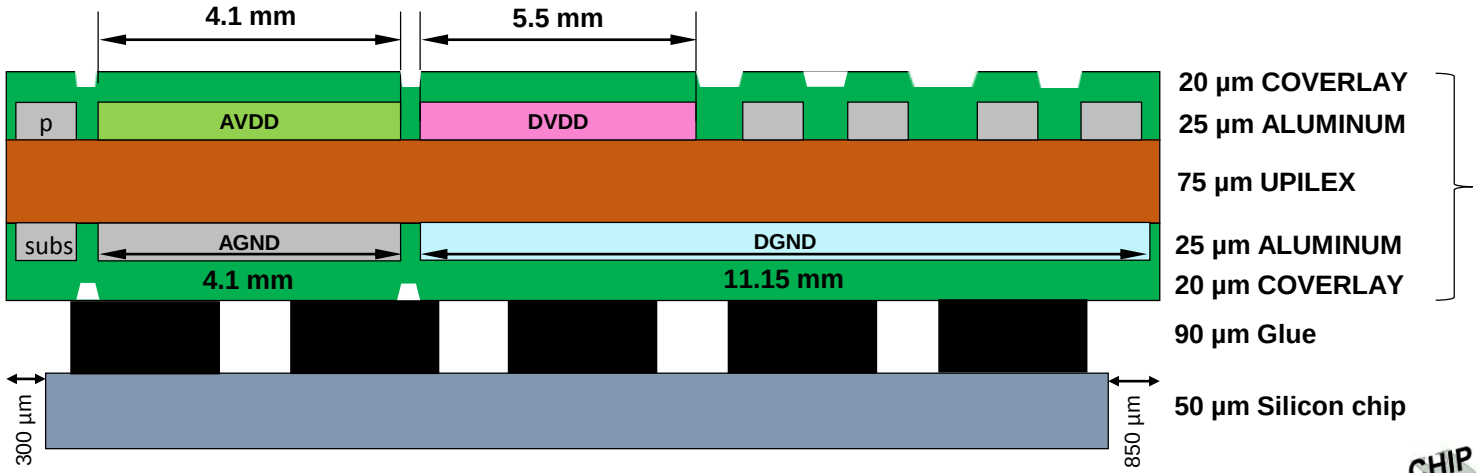
- Dimensional specifications

The design (**geometry of vias and interconnection pads, location of SMD components, solder mask opening**) has been optimized wrt the preliminary layout presented at the EDR, in order to allow reliable automated wire bonding using 3 wires per connection.

Position tolerance of ± 40 µm is required to align vias on sensor interconnection pads by overlapping the FPC on the pixel chips using nominal positions provided by alignment pin-holes.

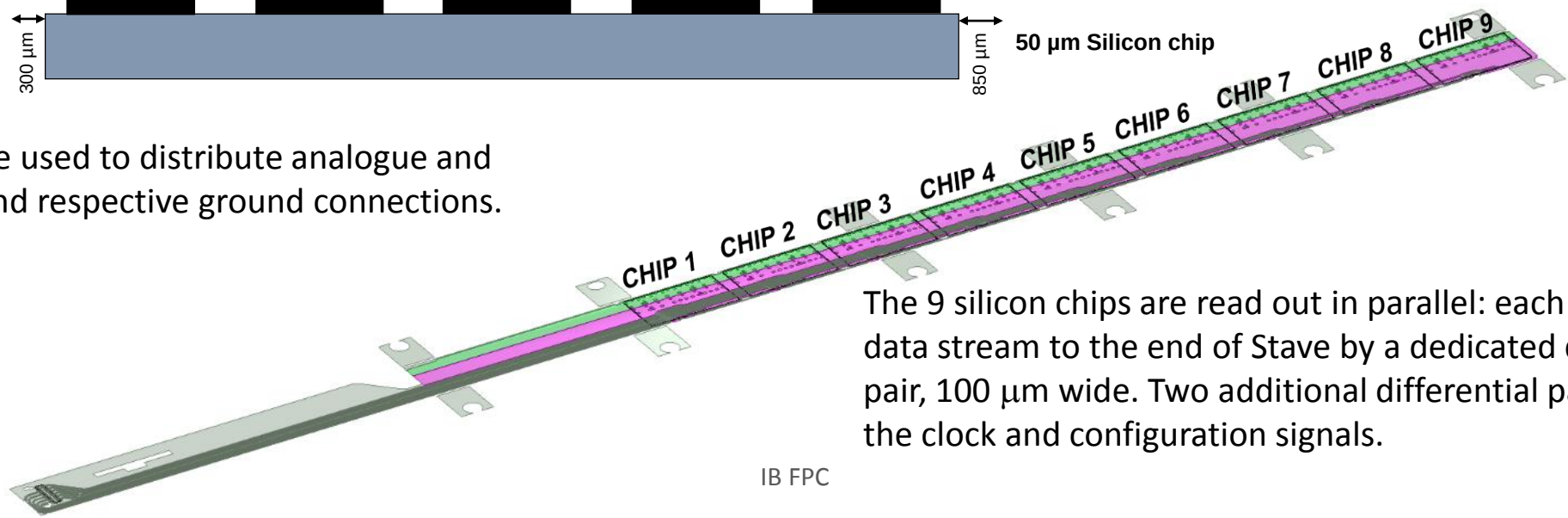
IB FPC Layout





20 µm COVERLAY
25 µm ALUMINUM
75 µm UPILEX
25 µm ALUMINUM
20 µm COVERLAY
165 µm
90 µm Glue
50 µm Silicon chip

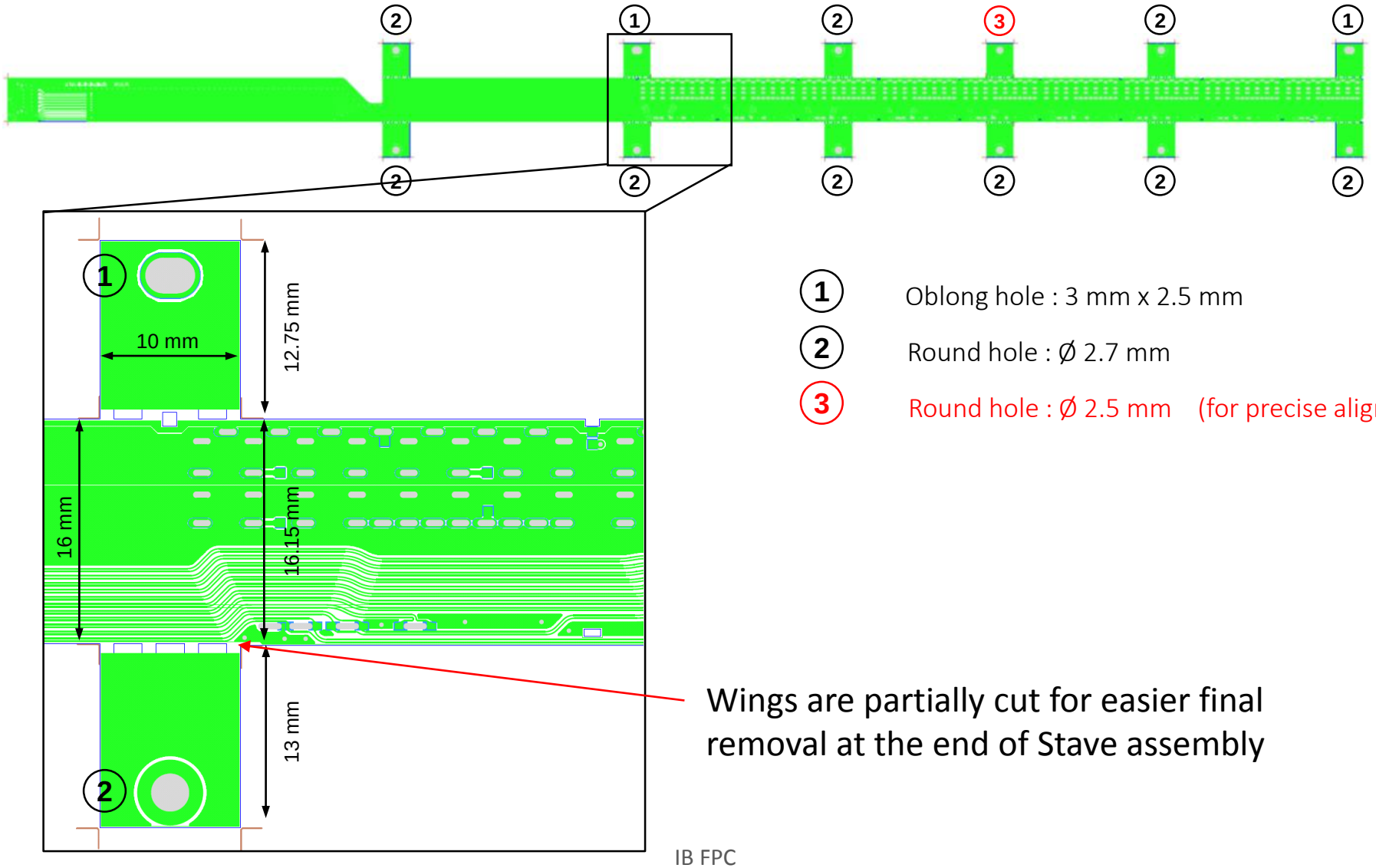
Large planes are used to distribute analogue and digital power and respective ground connections.



The 9 silicon chips are read out in parallel: each chip sends its data stream to the end of Stave by a dedicated differential pair, 100 µm wide. Two additional differential pairs distribute the clock and configuration signals.

IB FPC Layout

Alignment and handling wings



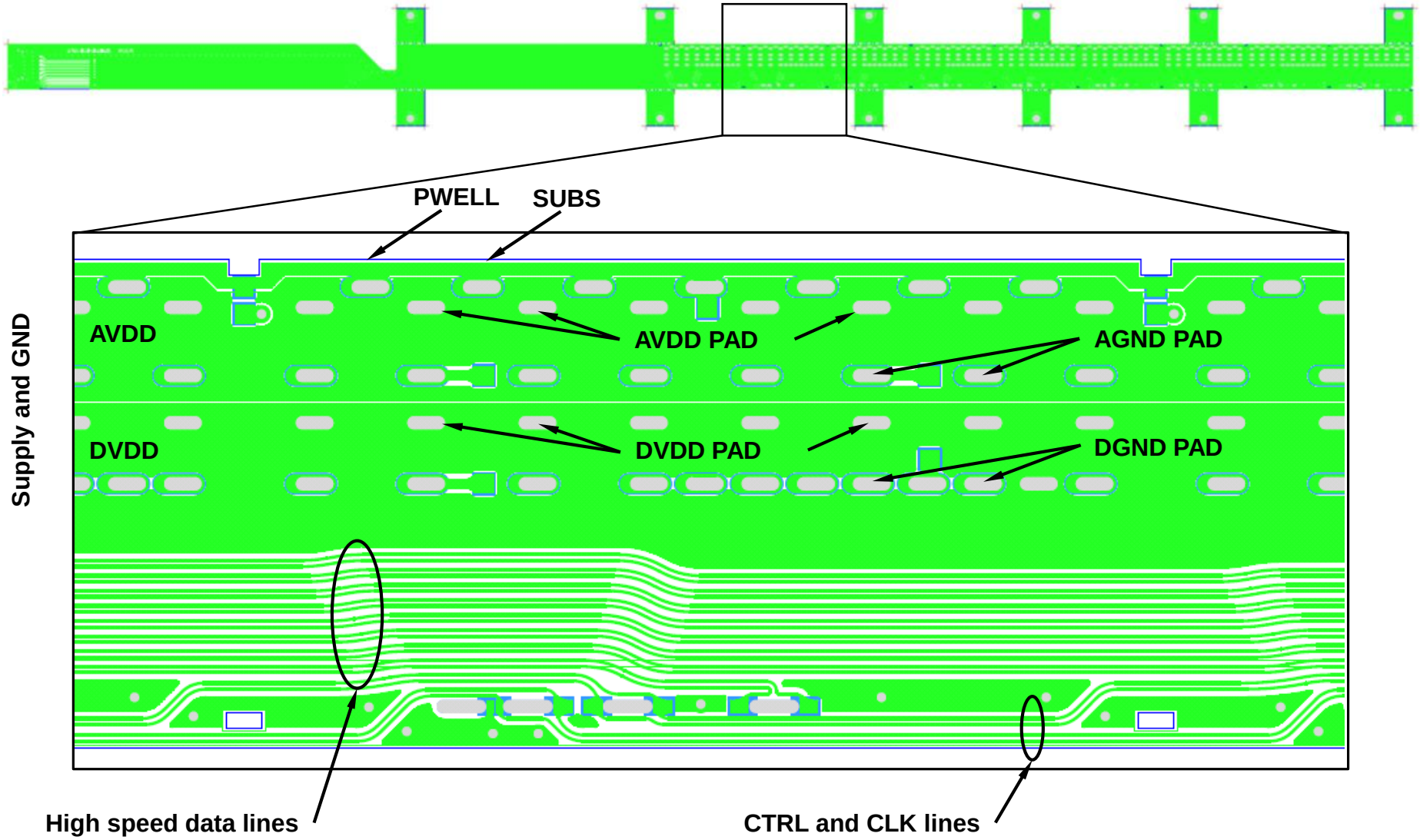
1 Oblong hole : 3 mm x 2.5 mm

2 Round hole : Ø 2.7 mm

3 Round hole : Ø 2.5 mm (for precise alignment)

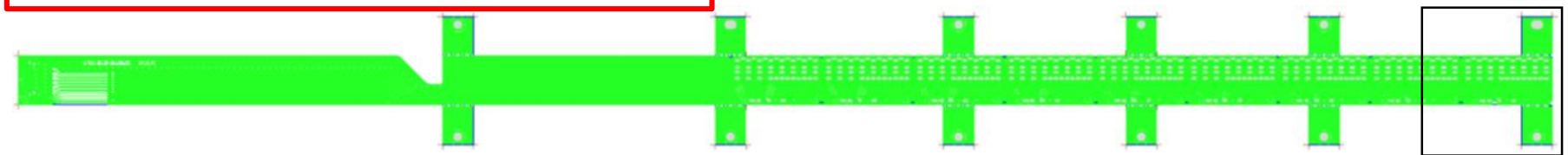
Wings are partially cut for easier final removal at the end of Stave assembly

IB FPC Layout

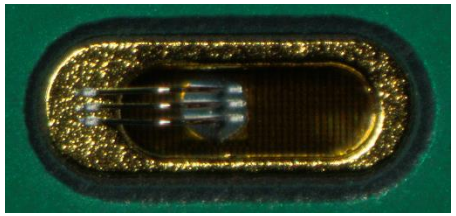


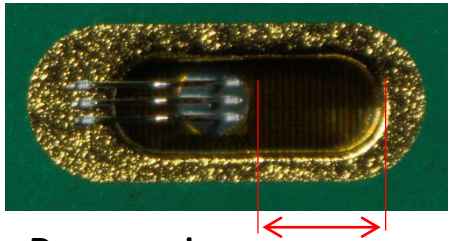
IB FPC Layout

GND and power supply vias, single pad

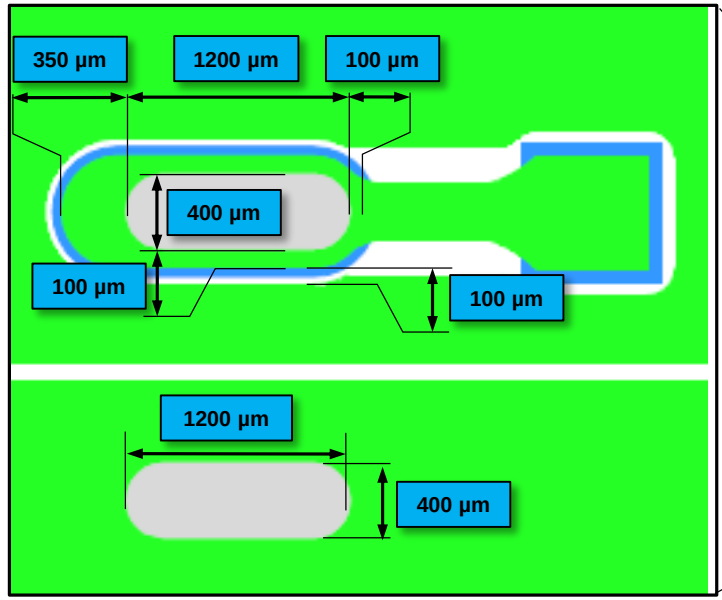


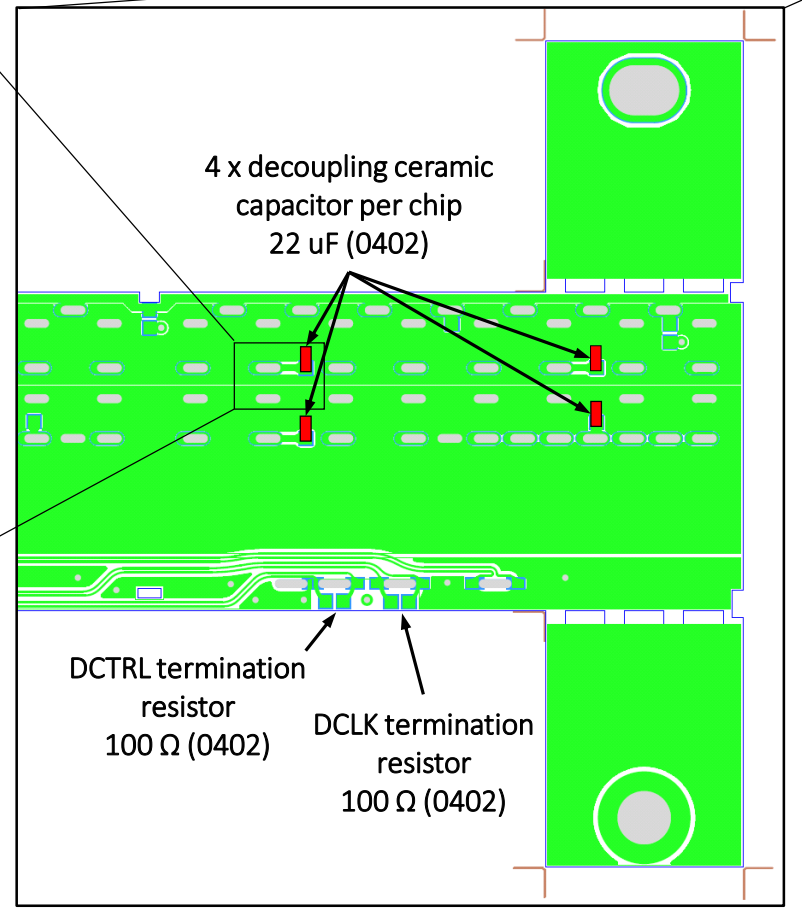
GND via





Power via

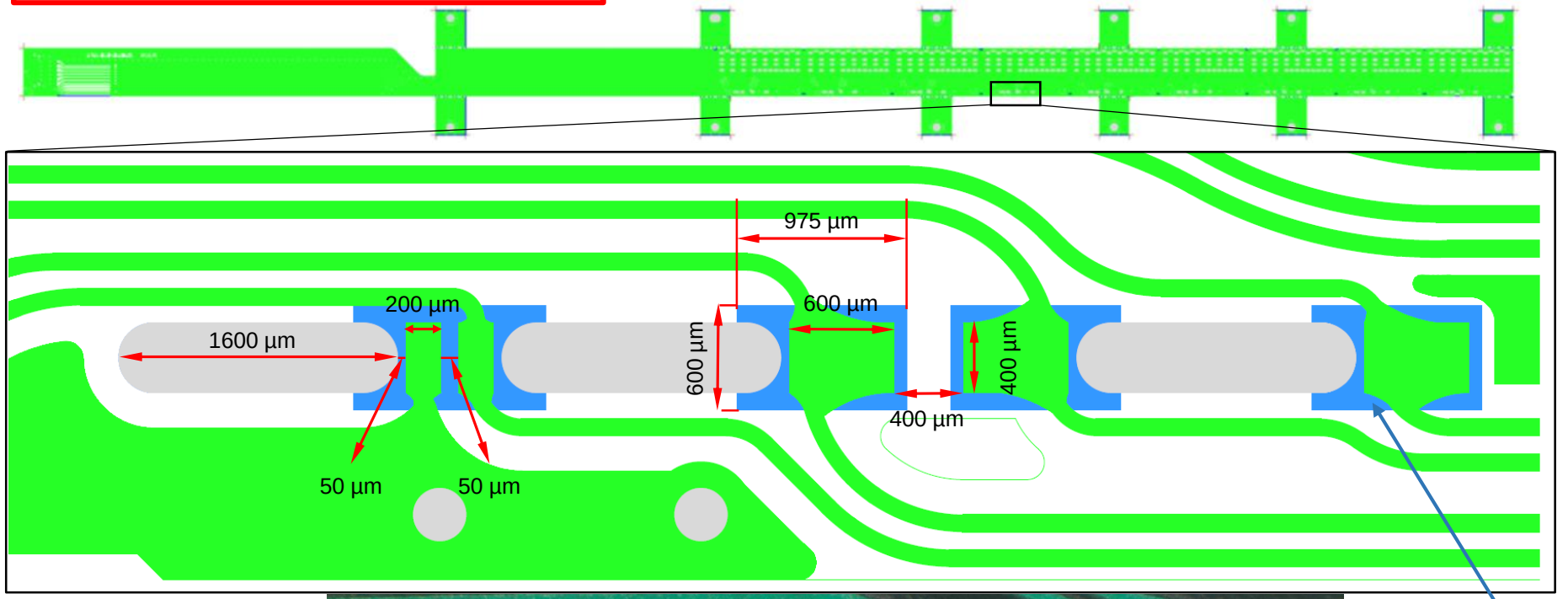




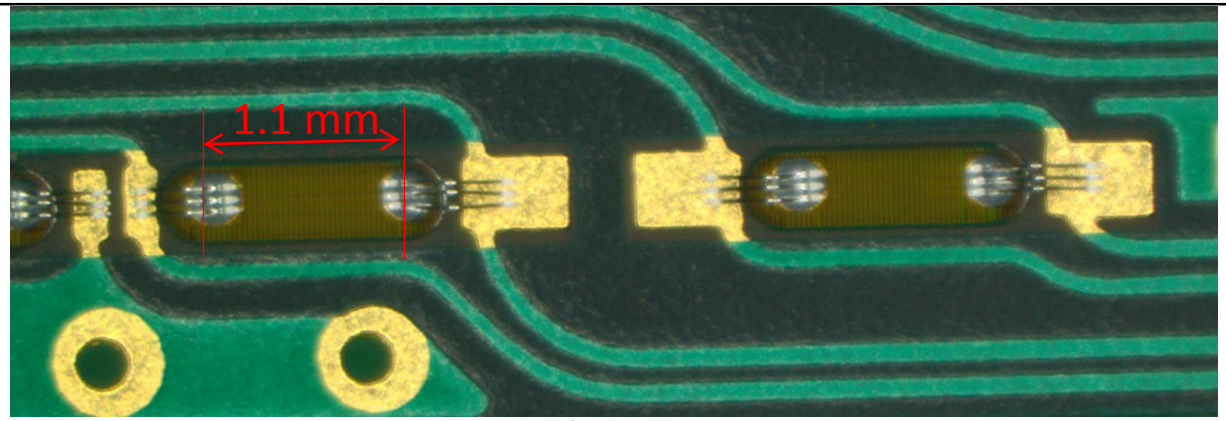
~ 0.7 mm : optimal clearance between chip pad edge and via edge for bonding machine head

IB FPC Layout

Control and data vias, double pad

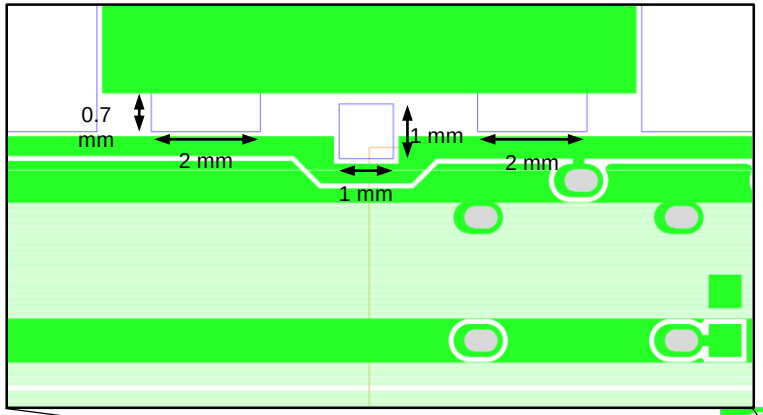


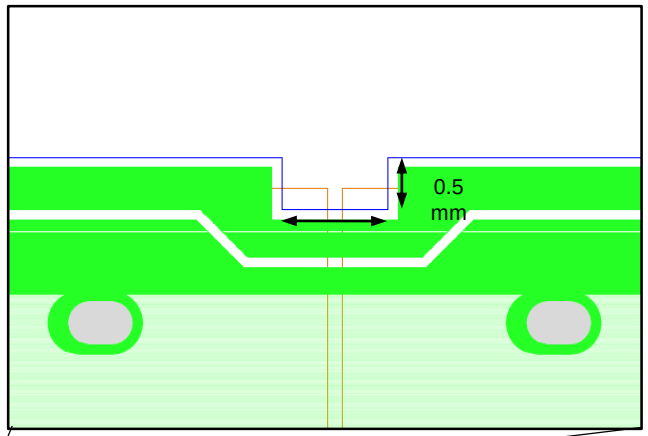
Gap between pads does not allow “single pad” via geometry: adopted double pad (and rotation of bonding head).

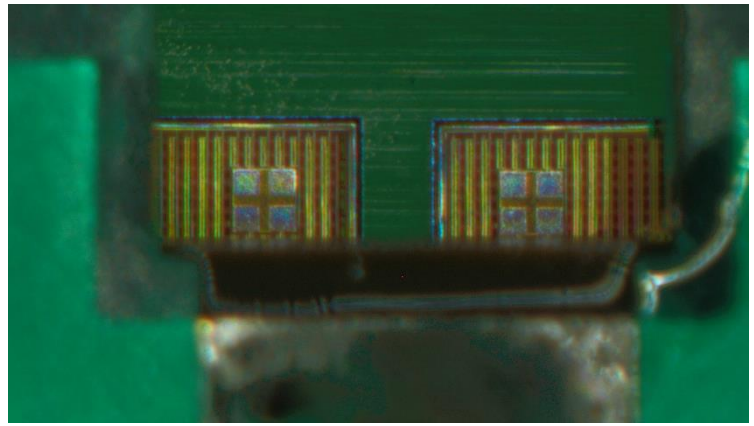


In blue: openings in the solder mask

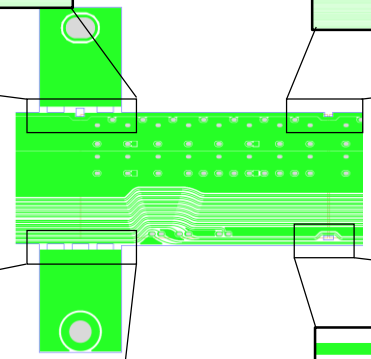
Inspection Slits

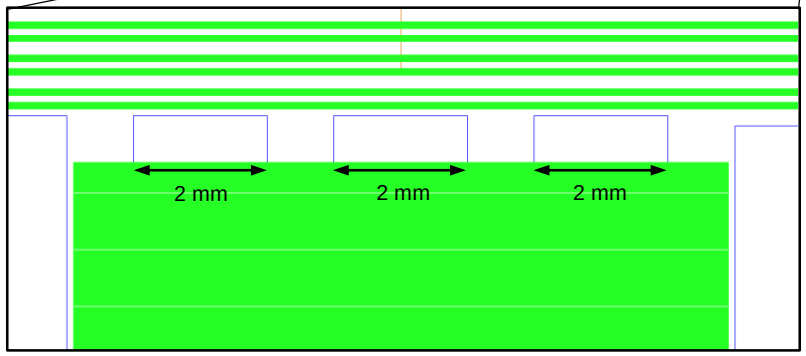


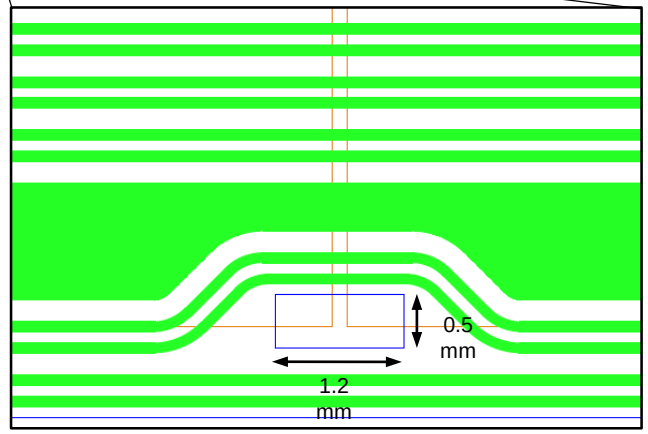


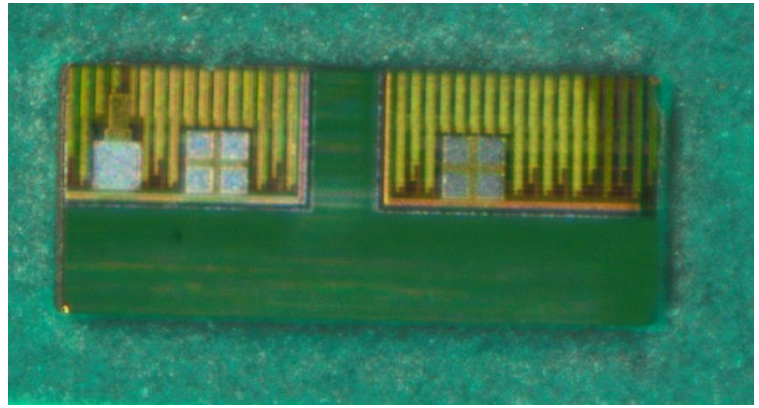


Inspection slits are implemented to verify and measure underlying chips position using reference marks



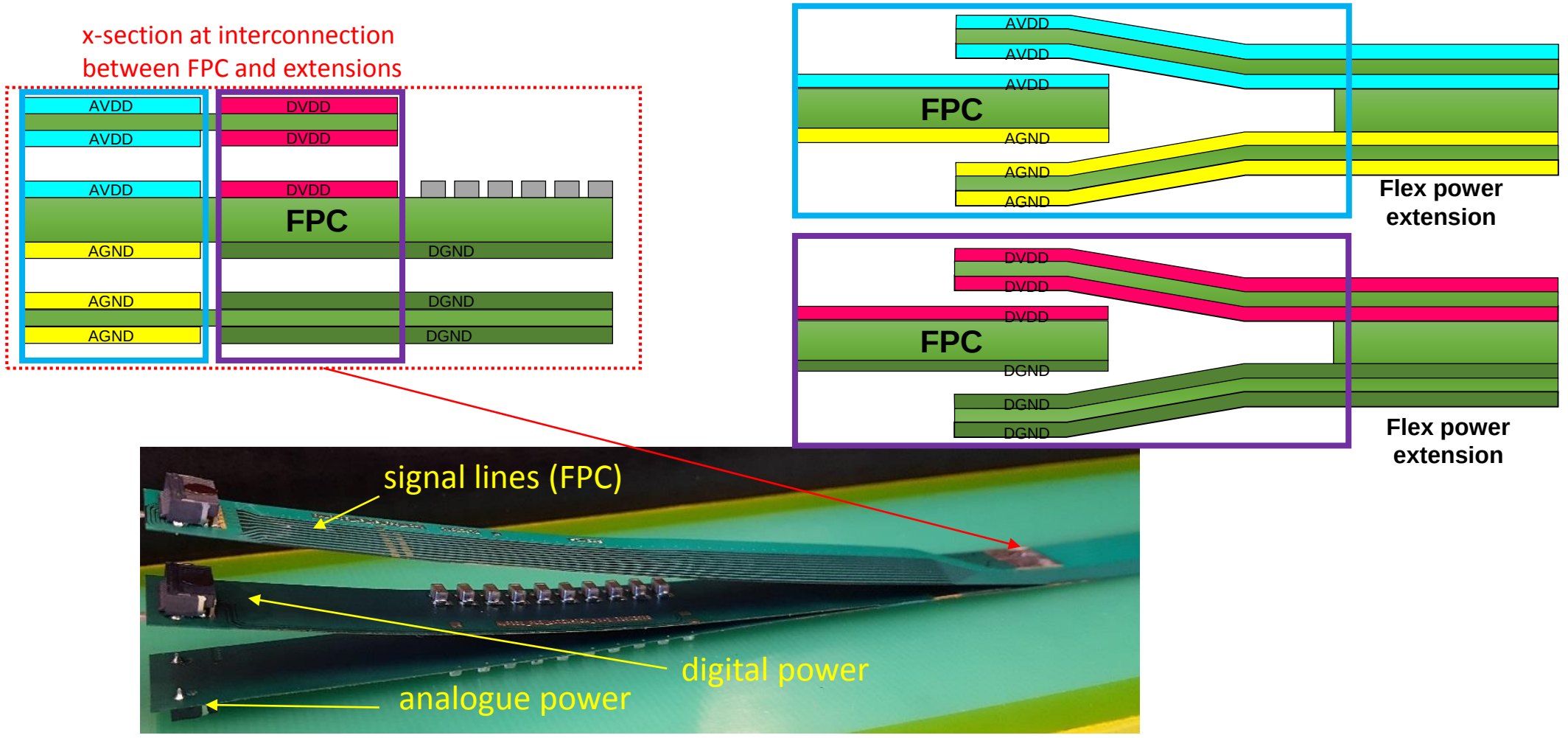






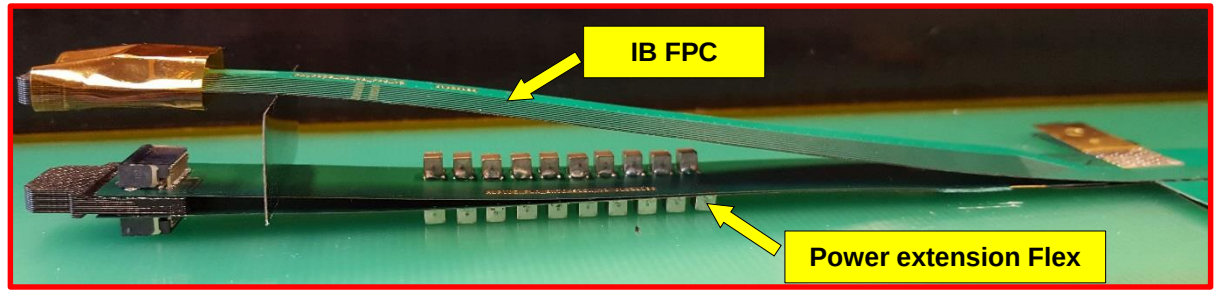
FPC Extension for Connection to Electrical Services

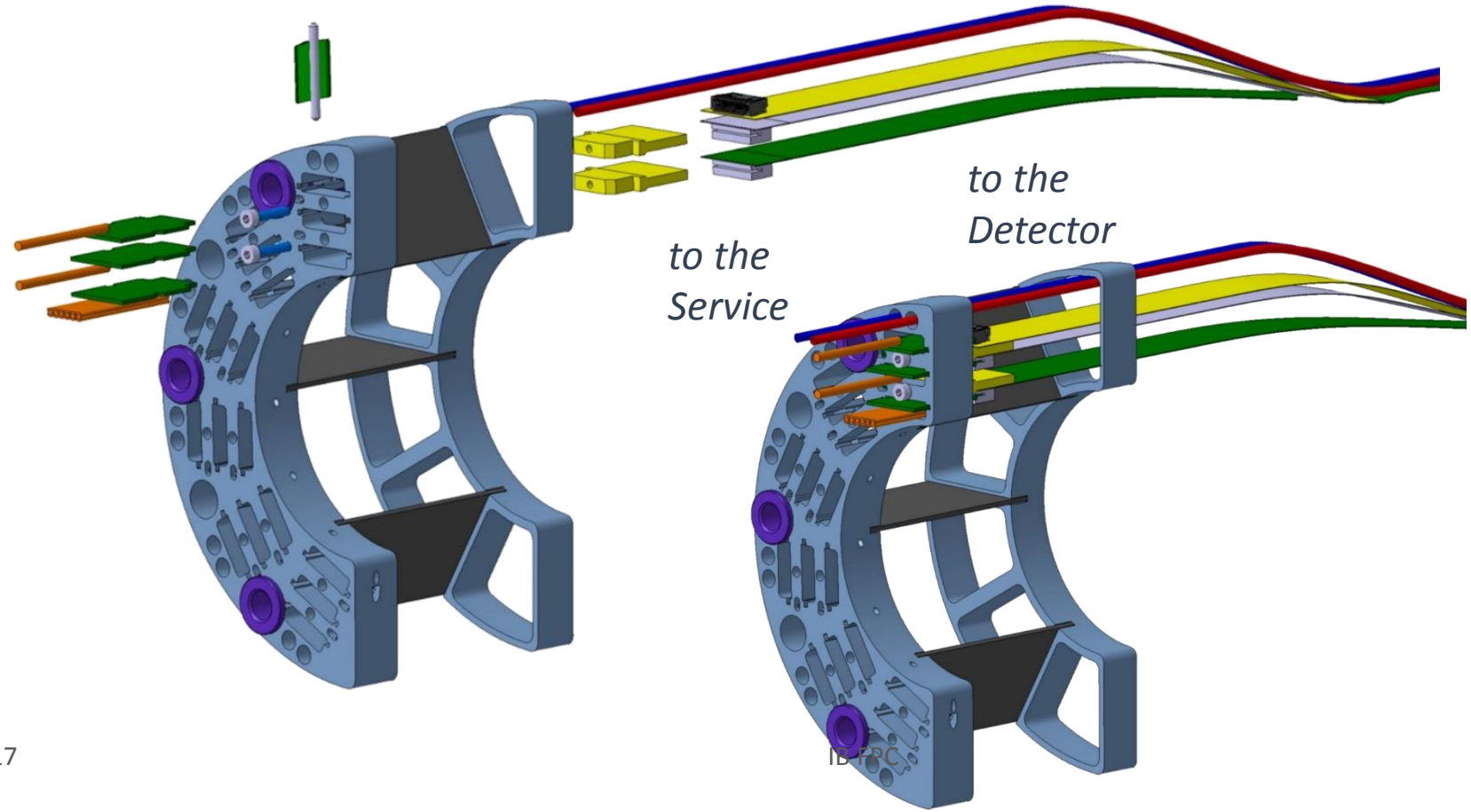
The connection to the service cables is achieved by a double FPC extension which is soldered to the HIC



FPC Extension for Connection to Electrical Services

Such extensions are equipped with passive components (10x 220 uF capacitors) to stabilize the analogue and digital power supplies, respectively

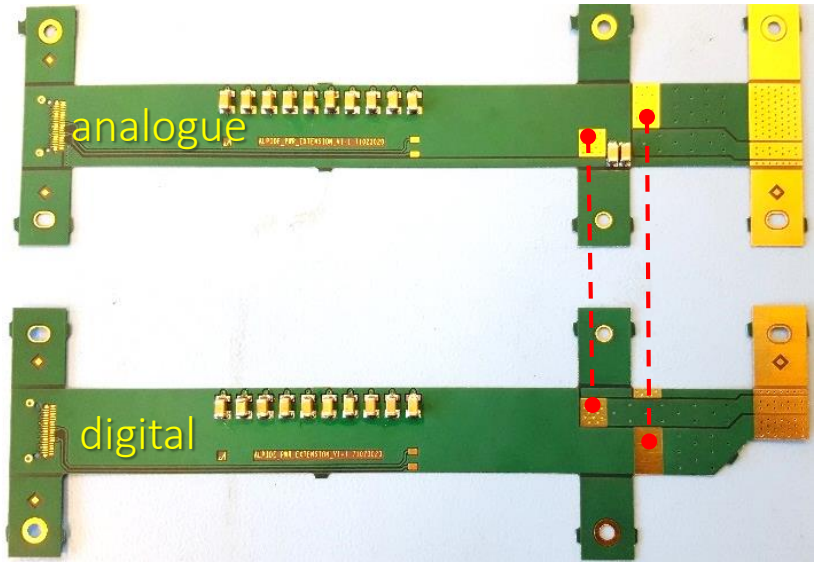


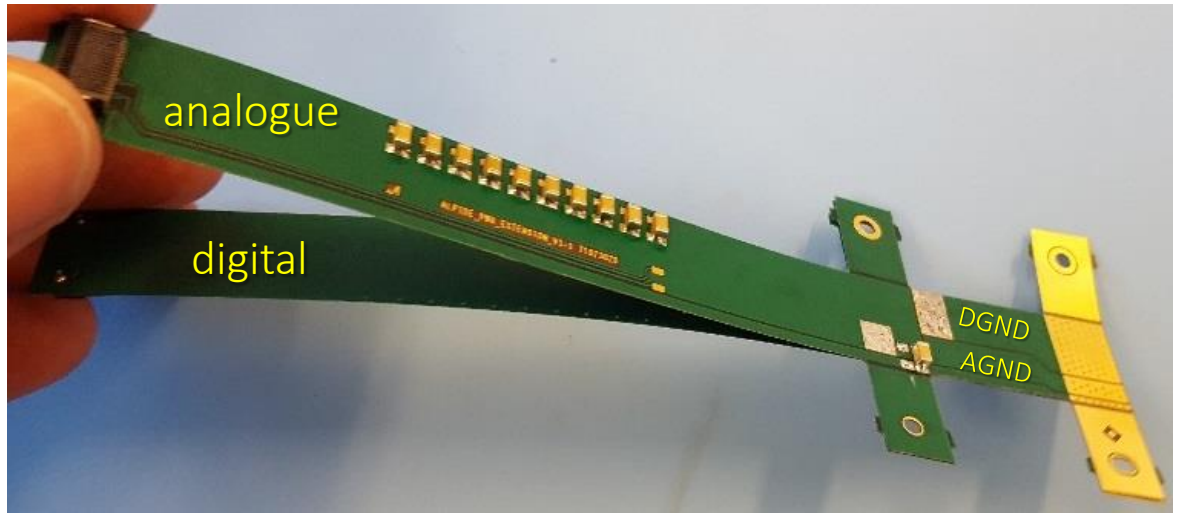


This solution allows to implement a “flexible” connection to external service cables with minimized space occupancy

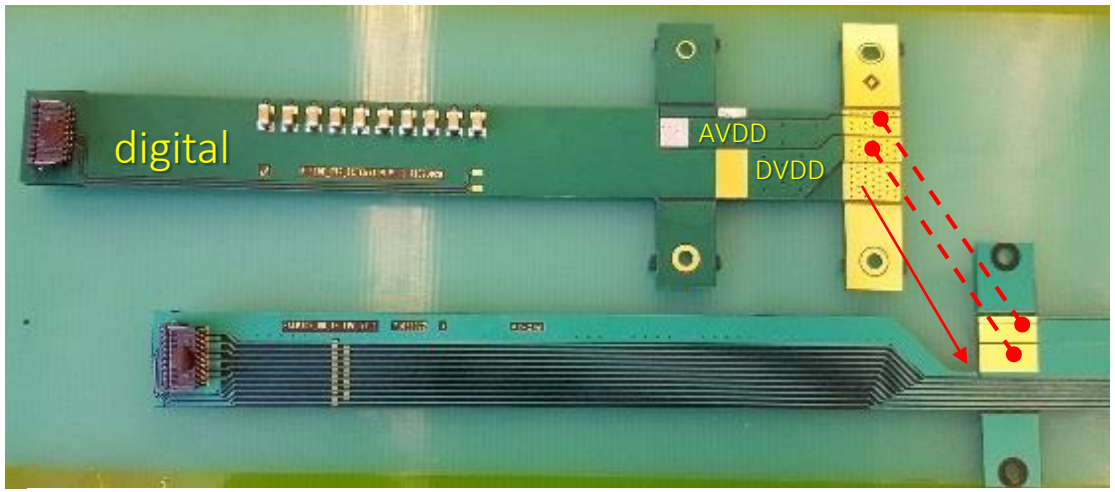
FPC Extension for Connection to Electrical Services

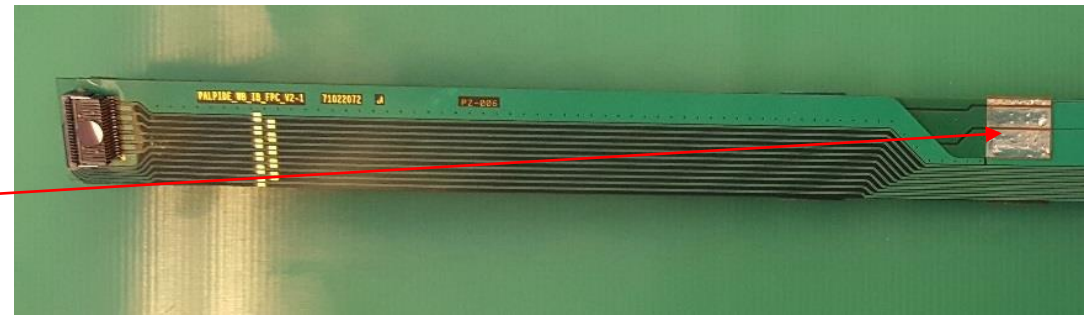
2-layer flex, PI: 50 µm, Cu: 35 µm, solder mask: 20 µm





The two flexes are connected together, AVDD is transferred from top to bottom





The PWR extension is connected to the FPC by iron soldering and wings are cut.

FPC

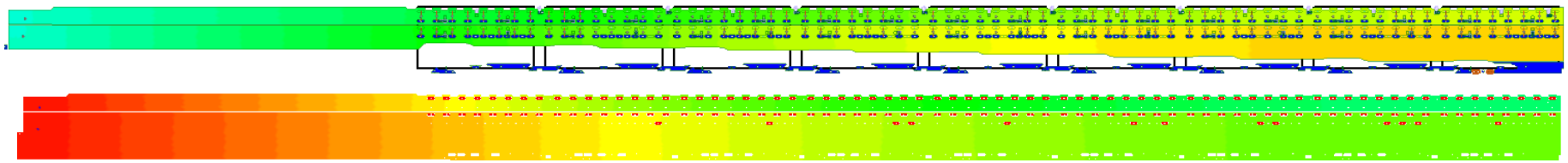
IB FPC Performance: Supply Voltage Drop

ANSYS simulation parameters

Nominal Supply Voltage (analogue and digital) => 1.8V
Chip area : 3cm x 1.5 cm => 4.5 cm^2
Chip power : 4.5 cm^2 x **45 mW/cm^2** => 202 mW

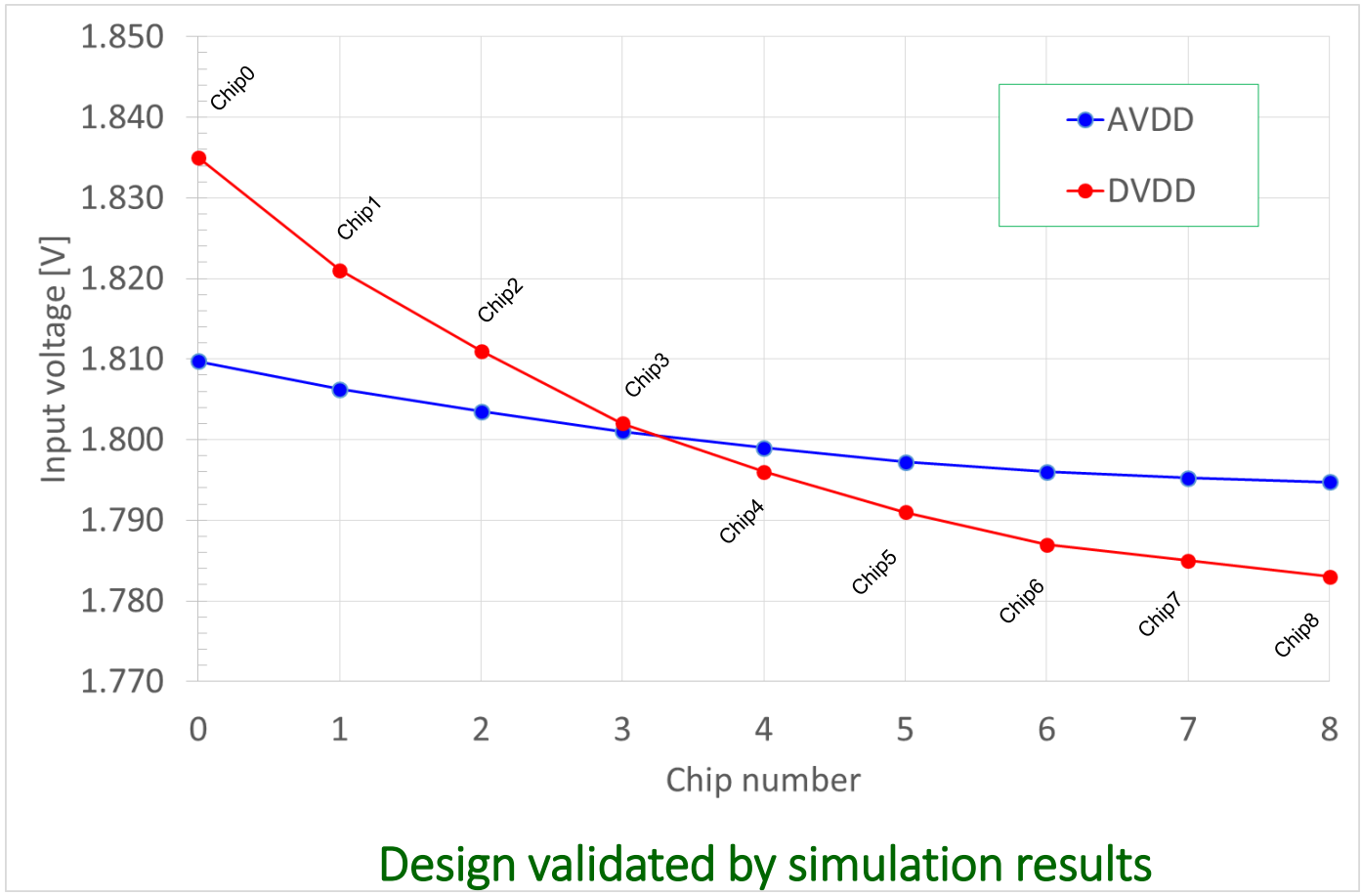
2/3 for digital : 180 mW / Chip
1/3 for analogue : 22 mW / Chip

IB FPC performance: power supply drop



Power plane, AVDD & DVDD DC Voltage drop

Ground plane, AGND & DGND DC Voltage drop



Design validated by simulation results

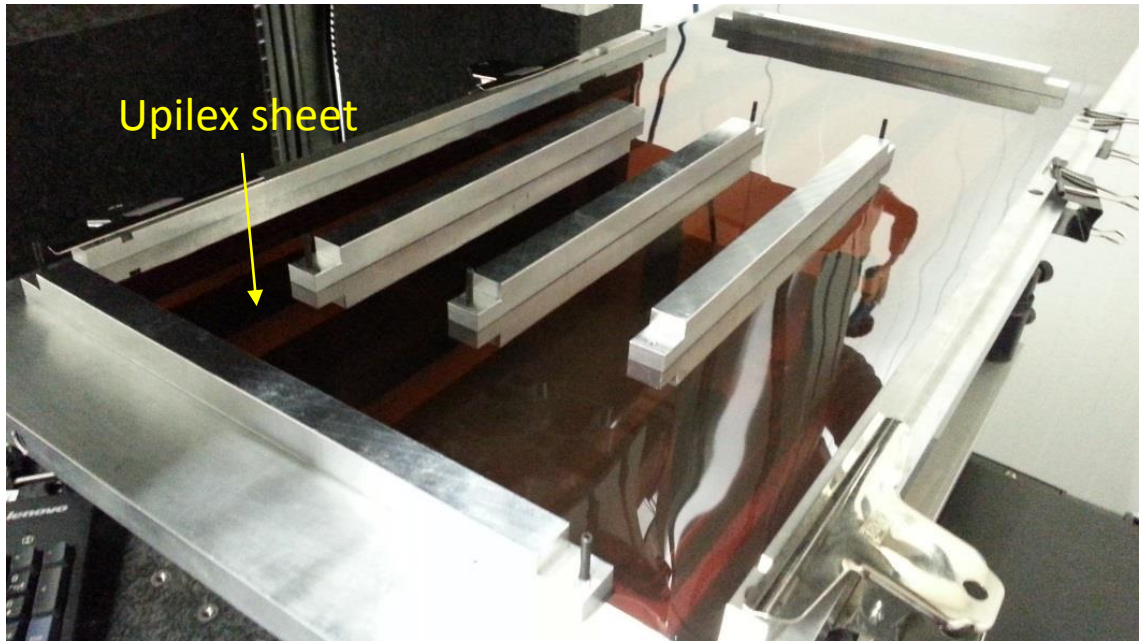
ANALOGUE	Mean	Voltage drop
Chip0	1.810V	+ 9.75 mV
Chip1	1.806V	+ 6.25 mV
Chip2	1.804V	+ 3.5 mV
Chip3	1.801V	+ 1 mV
Chip4	1.799V	- 1 mV
Chip5	1.797V	- 2.75 mV
Chip6	1.796V	- 4 mV
Chip7	1.795V	- 4.75 mV
Chip8	1.795V	- 5.25 mV

DIGITAL	Mean	Voltage drop
Chip0	1.835V	+ 35 mV
Chip1	1.821V	+ 21 mV
Chip2	1.811V	+ 11 mV
Chip3	1.802V	+ 2 mV
Chip4	1.796V	- 4 mV
Chip5	1.791V	- 9 mV
Chip6	1.787V	- 13 mV
Chip7	1.785V	- 15 mV
Chip8	1.783V	- 17 mV

IB FPC Manufacturing Procedure

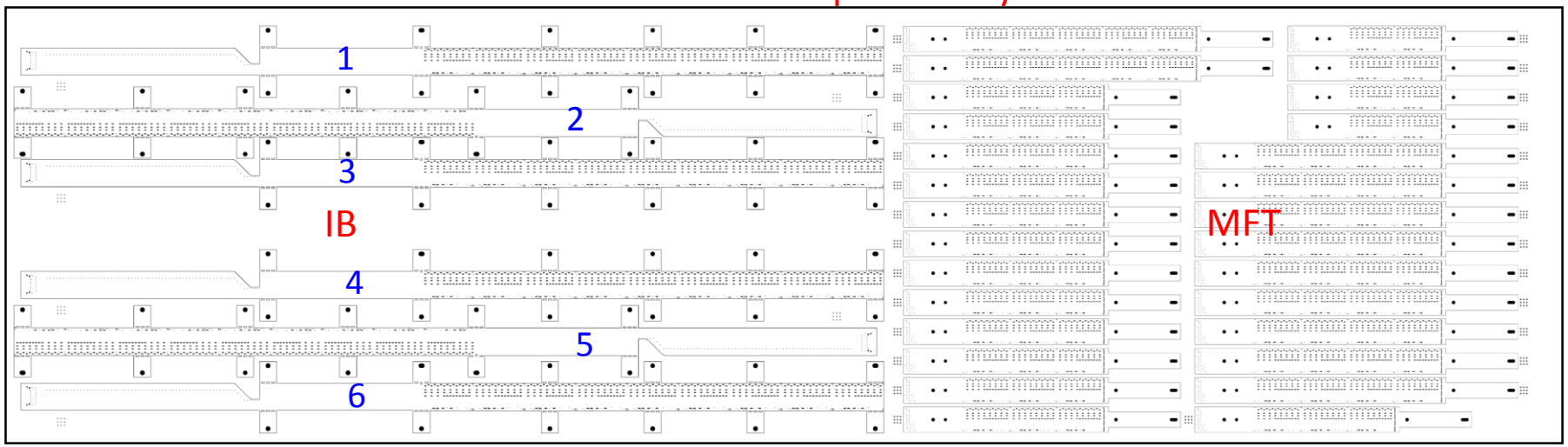
step	conditions	place	validation
1 . Thermal stabilisation of Upilex-75S sheets	2 h at 400 °C and 1E-08 mbar	CERN or Bodycote (F)	Visual inspection
2. Holes drilling by laser	23 +/- 1 °C (Upilex-75S CTE 20 ppm)	KIRANA (IT)	Metrology (dimensional)
3. Preparation for Al coating: cleaning, light polishing in sand blasting machine	3 passages at 1.5 bar, 0.2 m/s, pumice powder coarse FF 10-177 um	CERN	Metrology (witness samples surface roughness)
4. Al PVD coating	12 h of vacuum P < 10E-08 before starting	HEF (F)	Peel test, R^2 measurement, Al thickness on witness samples
5. LDI, etching, Ni/Au, solder mask coverlay		CERN	Visual inspection, electrical continuity, resistivity measurements, metrology, metal layers thickness, “bondability” test
6. SMD components mounting by hand (baseline); evaluation of vapour phase reflow oven @ 160 °C in progress	Sn-Pb solder paste,	CERN	Visual inspection
7. Cleaning	isopropyl alcohol ultrasonic bath 3’	CERN	Visual inspection, electrical continuity, resistivity measurements
8. Storage in N2		CERN	

Laser Drilling



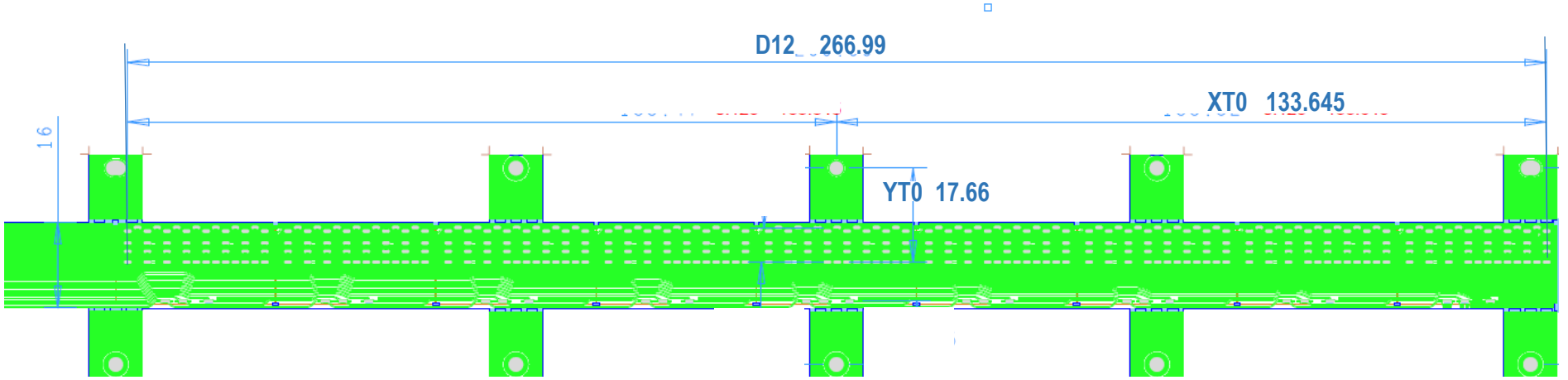
- Max four sheets of 95x28 cm^2 can be mounted in the PVD system performing the Al coating;
- The layout has been optimized in order to maximize the number of FPC/sheet, a 7^{th} FPC will be added in the middle
- Production is shared with MFT Upgrade project

Hole pattern layout



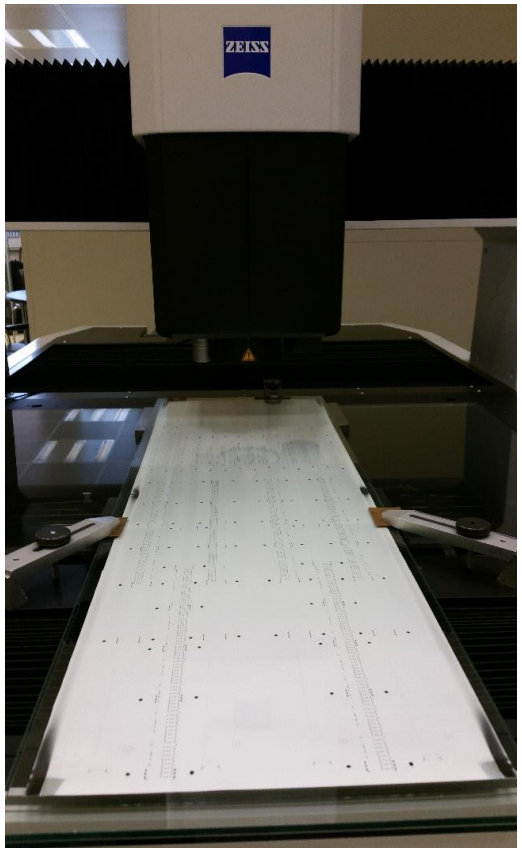
FPC Metrology Results

- The holes pattern has been designed to compensate the residual shrinking observed after Al coating (~ 0.14 %) induced by cooling down of deposited Al layers
- Reference values:
  - Distance (D12) between first and last via of central row in each FPC
  - Position (XT0, YT0) of reference hole used for alignment wrt to first via



QUOTE	nominal value [mm]	Compensated value [mm]
D12	266.990	267.364
XT0	133.645	133.830
YT0	17.660	17.684

FPC Metrology Results

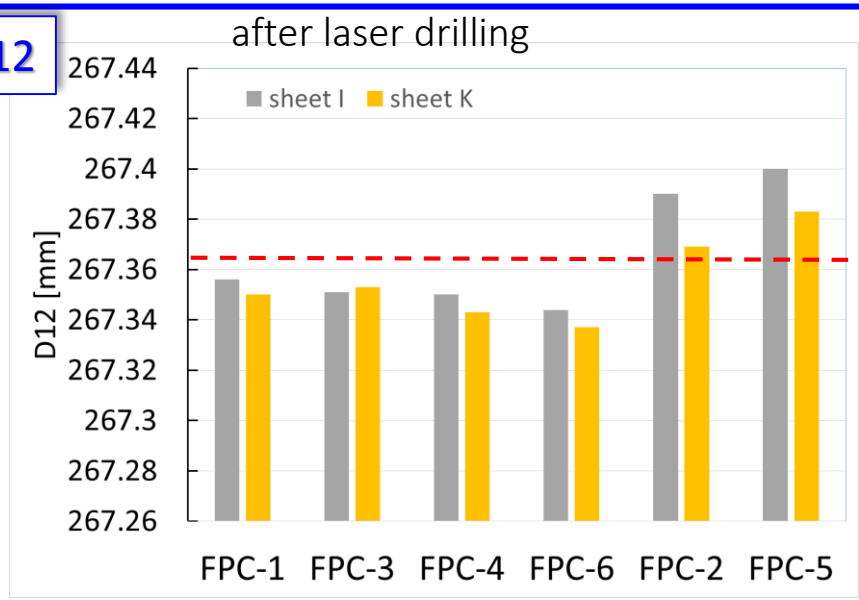


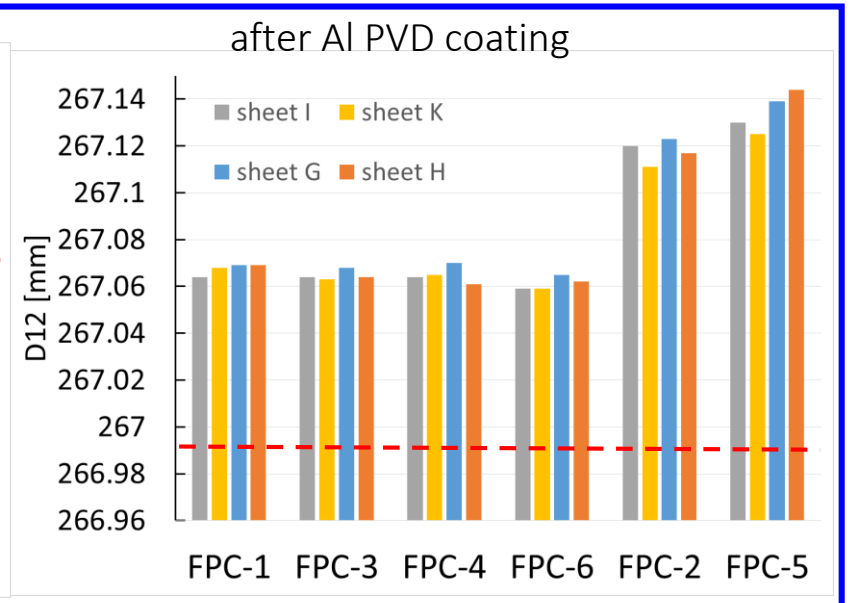
FPC thickness

- Typical st. dev in one FPC ~ 4 um
- On a sample of 12 pieces:

avg: 167.7 um, st. dev. 2.8 um

D12





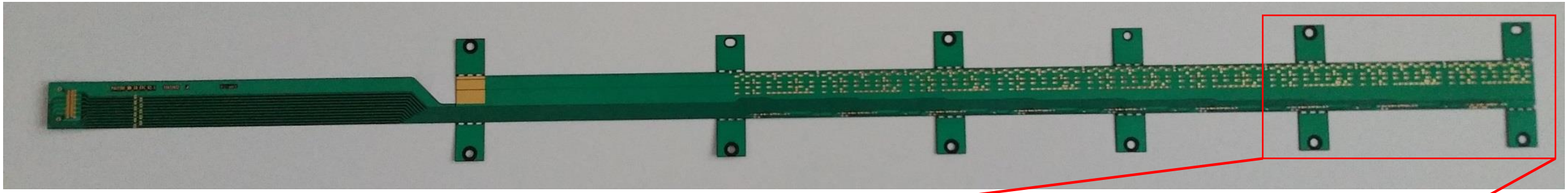
Avg/stdev	I+K (1,3,4,6)	I+K (2,5)	G+H (1,3,4,6)	G+H (2,5)	PZ+PX (1,3,4,6)	PZ+PX (2,5)
After laser drilling	267.35/0.006	267.39/0.01			267.35/0.01	267.40/0.01
After Al coating	267.06/0.003	267.12/0.007	267.07/0.003	267.13/0.012	267.02/0.003	267.087/0.01
Finished FPC					267.08/0.015	267.16/0.013

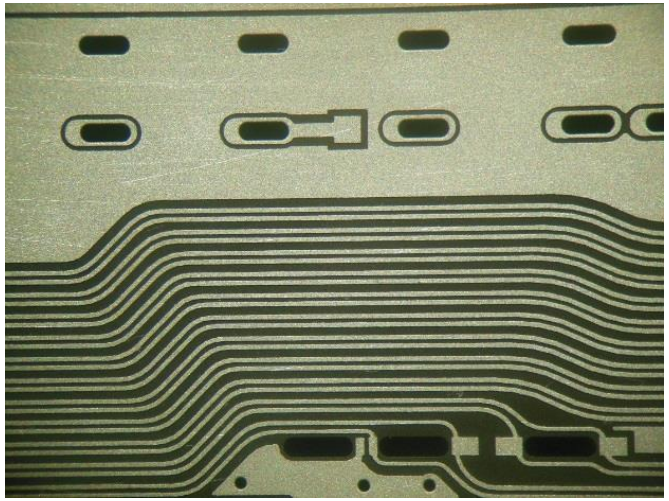
- FPC (2, 5) longer than FPC (1, 3, 4, 6) by ~ 60-80 um
- Finished FPCs (1, 3, 4, 6) are longer than nominal by ~80 um
- St. dev. ~ 15 um

➡ Fine tune shrink correction to achieve ± 40 um

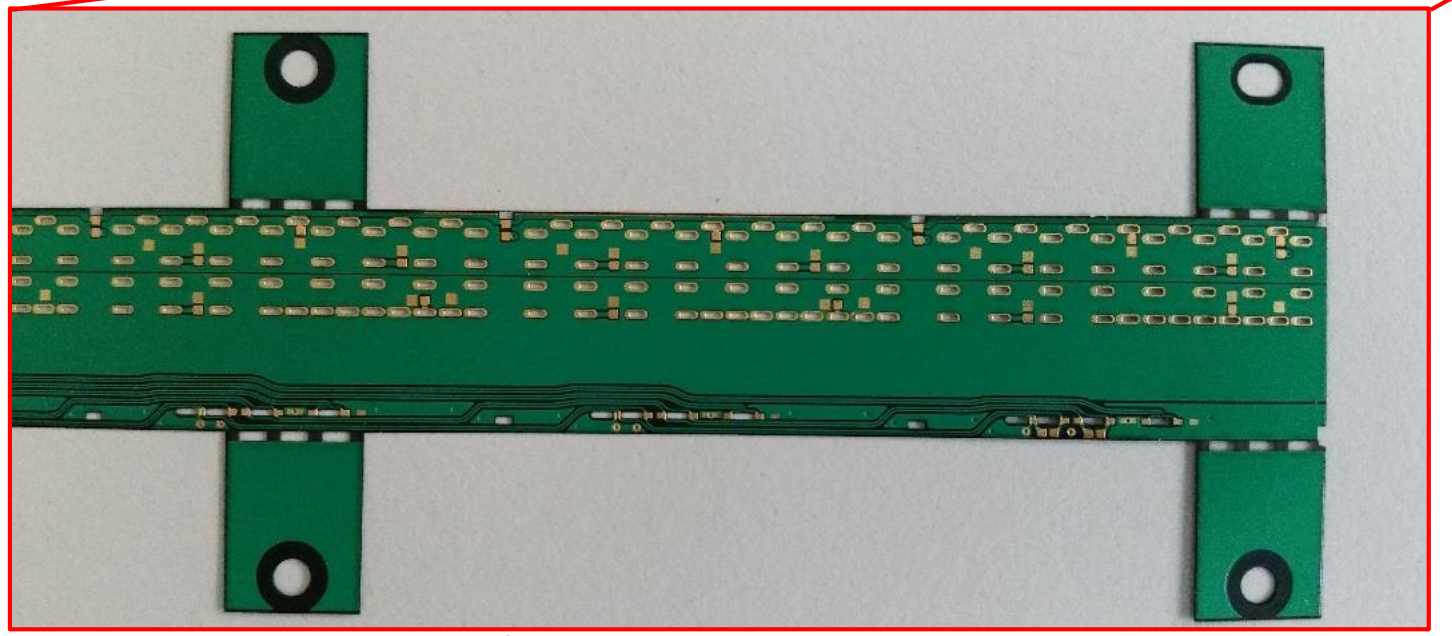
Prototypes Production

- Layout and processing have been optimized during all 2016 (more than 40 prototypes produced)
- In 2017 we procured 24 prototypes, yield ~ 80 %





Al top layer after etching



Production Schedule

- Amount to be produced: two full IB (96) + 20% → 116 FPC
- Including a yield of 80% for FPC production and of 90% for HIC modules production a total number of 160 FPC is required
- Each sheet contains 7 FPC, a total of 6 batches of 4 sheets need to be processed
- The estimated time for full production (started in March) is 9 months, completion of 48 FPC (for IB-1) expected for mid August

Production Schedule

	Task Name	Duration	Start	Finish
1				
2				
3	cut of Upilex-S75 sheets 950x280 , 24 pieces	1 day	Mon 13/02/17	Mon 13/02/17
4	thermal treatment at 400 C for 2 h of 24 sheets	10 days	Tue 14/02/17	Mon 27/02/17
5	**laser drilling 4 sheets**	**7 days**	**Thu 16/03/17**	**Fri 24/03/17**
6	metrology: dimensional, position batch 1	2 days	Mon 27/03/17	Tue 28/03/17
7	***preparation for Al coating: sand blasting, drying***	3 days	Wed 29/03/17	Fri 31/03/17
8	roughness measurement of witness sample	1 day	Mon 03/04/17	Mon 03/04/17
9	Al PVD coating @ HEF	5 days	Tue 04/04/17	Mon 10/04/17
10	metrology: dimensional	2 days	Tue 11/04/17	Wed 12/04/17
11	Al thickness and R check	1 day	Thu 13/04/17	Thu 13/04/17
12	**Processing batch #1**	**29 days**	**Fri 14/04/17**	**Wed 24/05/17**
13	LDI, Ag paste, etching, Ni/Au ...	18 days	Fri 14/04/17	Tue 09/05/17
14	laser cutting batch 1 IB + MFT	4 days	Wed 10/05/17	Mon 15/05/17
15	metrology: dimensional	4 days	Tue 16/05/17	Fri 19/05/17
16	SMD mount batch 1 IB + final check	3 days	Mon 22/05/17	Wed 24/05/17
17	**Processing batch #2**	**26 days**	**Mon 22/05/17**	**Mon 26/06/17**
18	SMD mount batch 2 IB + final check	3 days	Tue 27/06/17	Thu 29/06/17
19	**laser drilling 20 sheets**	**14 days**	**Mon 22/05/17**	**Thu 08/06/17**
20	metrology: dimensional, position batches 2, 3, 4, 5 and 6	2 days	Fri 09/06/17	Mon 12/06/17
21	***preparation for Al coating: sand blasting, drying***	5 days	Tue 13/06/17	Mon 19/06/17
22	roughness measurement of witness sample	1 day	Tue 20/06/17	Tue 20/06/17
23	Al PVD coating @ HEF	10 days	Wed 21/06/17	Tue 04/07/17
24	metrology: dimensional	2 days	Wed 05/07/17	Thu 06/07/17
25	Al thickness and R check	1 day	Fri 07/07/17	Fri 07/07/17
26	**Processing batch #3**	**26 days**	**Mon 10/07/17**	**Mon 14/08/17**
27	SMD mount batch 2 IB + final check	3 days	Tue 15/08/17	Thu 17/08/17
28	**Processing batch #4**	**26 days**	**Tue 15/08/17**	**Tue 19/09/17**
29	SMD mount batch 3 IB + final check	3 days	Wed 20/09/17	Fri 22/09/17
30	**Processing batch #5**	**26 days**	**Wed 20/09/17**	**Wed 25/10/17**
31	SMD mount batch 4 IB + final check	3 days	Thu 26/10/17	Mon 30/10/17
32	**Processing batch #6**	**26 days**	**Thu 26/10/17**	**Thu 30/11/17**
33	SMD mount batch 5 IB + final check	3 days	Fri 01/12/17	Tue 05/12/17