

power_control

Version: 1.0

Thursday 6th February, 2020 17:43

Control and monitor ALPIDE power. Interface several (up to 12, 2 for each stave) INA226 ICs via I2C.

1 Register List

#	Name	Mode	Address	Type	Length	Reset
0	config	RW	0x00000000	FIELDS	2	0x2
1	i2c_status	RO	0x00000001	FIELDS	8	0x0
2	i2c_write	RW	0x00000002	FIELDS	31	0x0
3	i2c_read	RO	0x00000003	FIELDS	16	0x0
4	i2c_command	PULSE	0x00000004	FIELDS	3	0x0
5	dvdd_enable	RW	0x00000005	SLV	6	0x0
6	avdd_enable	RW	0x00000006	SLV	6	0x0
7	avdd_current_limits	RW	0x00000007	FIELDS	32	0x0
8	dvdd_current_limits	RW	0x00000008	FIELDS	32	0x0
9	minimum_current	RW	0x00000009	FIELDS	32	0x0
10	current_stave0	RO	0x0000000A	FIELDS	32	0x0
11	current_stave1	RO	0x0000000B	FIELDS	32	0x0
12	current_stave2	RO	0x0000000C	FIELDS	32	0x0
13	current_stave3	RO	0x0000000D	FIELDS	32	0x0
14	current_stave4	RO	0x0000000E	FIELDS	32	0x0
15	current_stave5	RO	0x0000000F	FIELDS	32	0x0
16	stave_dvdd_status	RO	0x00000010	FIELDS	18	0x0
17	stave_avdd_status	RO	0x00000011	FIELDS	18	0x0
18	reset_stave_status	PULSE	0x00000012	SLV	6	0x0
19	bias_control	RW	0x00000013	SLV	2	0x0

2 Registers

Register 2.1: CONFIG - RW (0x00000000)
Power Control configuration.

31	unused	2	1	0	Reset
-			1	0	

mode 0 $\backslash(\backslash\text{to}\backslash)\sim$ configuration mode. 1 $\backslash(\backslash\text{to}\backslash)\sim$ continuous monitoring mode. In configuration mode, the I2C bus is controlled by the AXI bus.

auto_shutoff If set, monitors the INA226 alert pin and disables power supply if alerts occur or current exceeds critical level as defined by register.

Register 2.2: I2C_STATUS - RO (0x00000001)
I2C bus status.

31	unused	8	7	6	5	4	3	2	1	0	Reset
-			0	0	0	0	0	0	0	0	

transfer_in_progress An I2C-transfers is in progress.

transmitting_byte An I2C byte transmit is in progress.

receiving_byte An I2C byte receiving is in progress.

command_completed Last I2C command was completed.

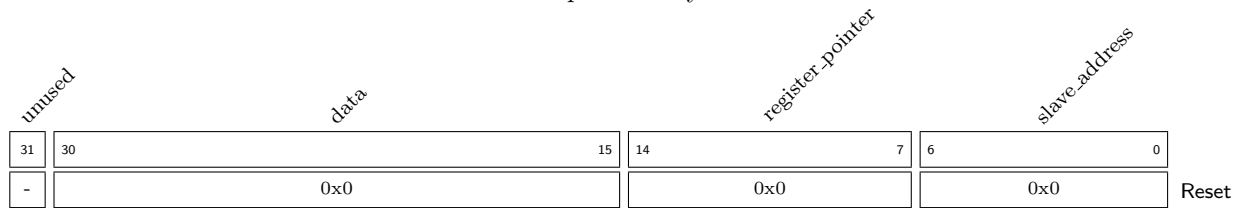
error Some kind of error occurred.

command_aborted I2C operation was aborted by user.

arbitration_lost I2C arbitration lost.

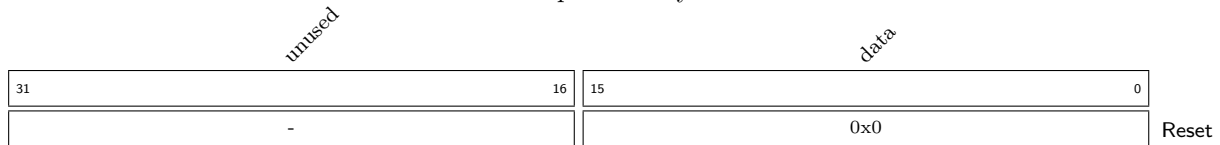
bus_busy I2C bus is busy.

Register 2.3: I2C_WRITE - RW (0x00000002)
I2C operation bytes.



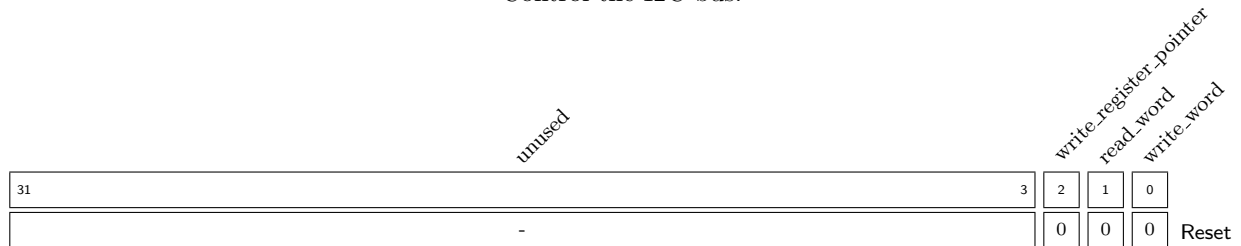
slave_address Slave-address byte.
register_pointer Register-pointer byte.
data Data to be written to device.

Register 2.4: I2C_READ - RO (0x00000003)
I2C operation bytes.



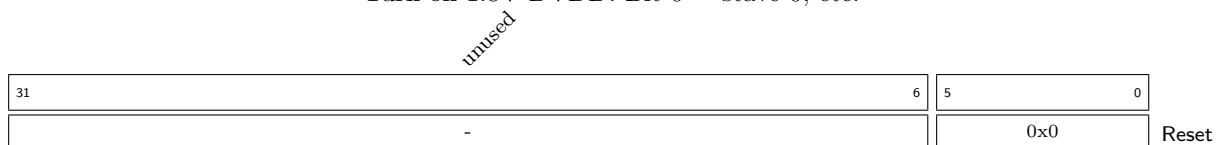
data Data read from device.

Register 2.5: I2C_COMMAND - PULSE FOR 1 CYCLES (0x00000004)
Control the I2C bus.



write_word Start I2C write procedure. Including register pointer and 2 bytes of data.
read_word Start I2C read procedure. Does not include writing of register pointer.
write_register_pointer Start I2C write register pointer procedure. Required to read a different register than what is already stored on the INA chips.

Register 2.6: DVDD_ENABLE - RW (0x00000005)
Turn on 1.8V DVDD. Bit 0 = stave 0, etc.



Register 2.7: AVDD_ENABLE - RW (0x00000006)
Turn on 1.8V AVDD. Bit 0 = stave 0, etc.

31	6	5	0
-		0x0	
			Reset

Register 2.8: AVDD_CURRENT_LIMITS - RW (0x00000007)
The current limits for the ALPIDE AVDD per stave. The resolution is set by settings on the INA226 chips.
Is ignored if the value is 0x0.

31	16	15	0
0x0		0x0	
			Reset

warning_threshold Current above this threshold triggers a warning.

critical_threshold Current above this threshold disables power regulator and triggers critical level.

Register 2.9: DVDD_CURRENT_LIMITS - RW (0x00000008)
The current limits for the ALPIDE AVDD per stave. The resolution is set by settings on the INA226 chips.
Is ignored if the value is 0x0.

31	16	15	0
0x0		0x0	
			Reset

warning_threshold Current above this threshold triggers a warning.

critical_threshold Current above this threshold disables power regulator and triggers critical level.

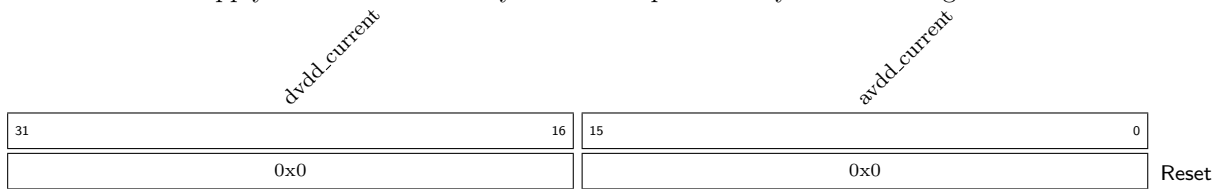
Register 2.10: MINIMUM_CURRENT - RW (0x00000009)
The minimum current of a stave. The resolution is set by settings on the INA226 chips. Is ignored if the value is 0x0.

31	16	15	0
0x0		0x0	
			Reset

dvdd Current below this threshold triggers a warning.

avdd Current below this threshold triggers a warning.

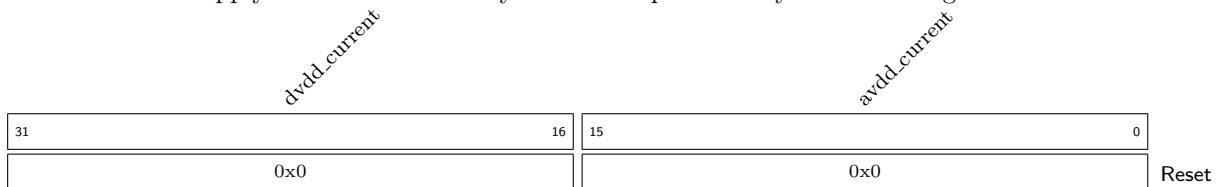
Register 2.11: CURRENT_STAVE0 - RO (0x0000000A)
Supply current measured by INA226. Updated only in monitoring mode.



avdd_current Analog supply current.

dvdd_current Digital supply current.

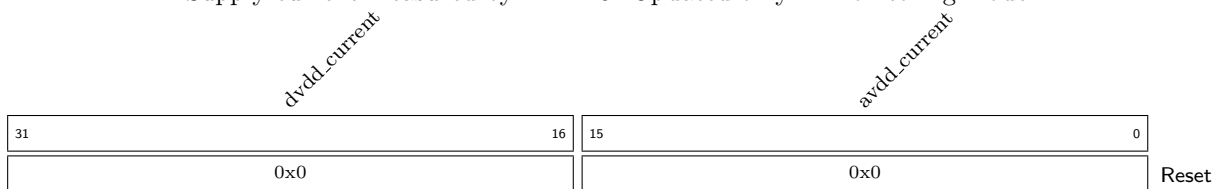
Register 2.12: CURRENT_STAVE1 - RO (0x0000000B)
Supply current measured by INA226. Updated only in monitoring mode.



avdd_current Analog supply current.

dvdd_current Digital supply current.

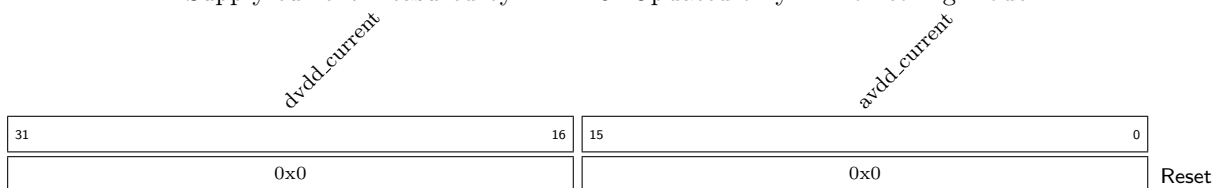
Register 2.13: CURRENT_STAVE2 - RO (0x0000000C)
Supply current measured by INA226. Updated only in monitoring mode.



avdd_current Analog supply current.

dvdd_current Digital supply current.

Register 2.14: CURRENT_STAVE3 - RO (0x0000000D)
Supply current measured by INA226. Updated only in monitoring mode.



avdd_current Analog supply current.

dvdd_current Digital supply current.

Register 2.15: CURRENT_STAVE4 - RO (0x0000000E)
Supply current measured by INA226. Updated only in monitoring mode.

<i>dvdd_current</i>		<i>avdd_current</i>	
31	16	15	0
0x0		0x0	
Reset			

avdd_current Analog supply current.

dvdd_current Digital supply current.

Register 2.16: CURRENT_STAVE5 - RO (0x0000000F)
Supply current measured by INA226. Updated only in monitoring mode.

<i>dvdd_current</i>		<i>avdd_current</i>	
31	16	15	0
0x0		0x0	
Reset			

avdd_current Analog supply current.

dvdd_current Digital supply current.

Register 2.17: STAVE_DVDD_STATUS - RO (0x00000010)
Status of DVDD supply for each stave. 0 $\backslash(\backslash\text{to}\backslash)\sim$ OFF, 1 $\backslash(\backslash\text{to}\backslash)\sim$ OK, 2 $\backslash(\backslash\text{to}\backslash)\sim$ WARNING, 3 $\backslash(\backslash\text{to}\backslash)\sim$ CRITICAL, 4 $\backslash(\backslash\text{to}\backslash)\sim$ ALERT.

<i>unused</i>		<i>stave5</i>		<i>stave4</i>		<i>stave3</i>		<i>stave2</i>		<i>stave1</i>		<i>stave0</i>	
31	18	17	15	14	12	11	9	8	6	5	3	2	0
-		0x0		0x0		0x0		0x0		0x0		0x0	
Reset													

stave0 Stave0 DVDD status.

stave1 Stave1 DVDD status.

stave2 Stave2 DVDD status.

stave3 Stave3 DVDD status.

stave4 Stave4 DVDD status.

stave5 Stave5 DVDD status.

Register 2.18: STAVE_AVDD_STATUS - RO (0x00000011)

Status of AVDD supply for each stave. 0 $\backslash(\backslash\text{to}\backslash)\sim$ OFF, 1 $\backslash(\backslash\text{to}\backslash)\sim$ OK, 2 $\backslash(\backslash\text{to}\backslash)\sim$ WARNING, 3 $\backslash(\backslash\text{to}\backslash)\sim$ CRITICAL, 4 $\backslash(\backslash\text{to}\backslash)\sim$ ALERT.

<i>unused</i>		<i>stave5</i>		<i>stave4</i>		<i>stave3</i>		<i>stave2</i>		<i>stave1</i>		<i>stave0</i>	
31	18	17	15	14	12	11	9	8	6	5	3	2	0
-		0x0		0x0		0x0		0x0		0x0		0x0	

Reset

stave0 Stave0 AVDD status.

stave1 Stave1 AVDD status.

stave2 Stave2 AVDD status.

stave3 Stave3 AVDD status.

stave4 Stave4 AVDD status.

stave5 Stave5 AVDD status.

Register 2.19: RESET_STAVE_STATUS - PULSE FOR 1 CYCLES (0x00000012)

Resets staves num status.

<i>unused</i>		<i>stave0</i>	
31	6	5	0
-		0x0	

Reset

Register 2.20: BIAS_CONTROL - RW (0x00000013)

Set the BIAS VOLTAGE for all staves. 00 $\backslash(\backslash\text{to}\backslash)\sim$ 0V, 01 $\backslash(\backslash\text{to}\backslash)\sim$ -2V1, 10 $\backslash(\backslash\text{to}\backslash)\sim$ -3V, 11 $\backslash(\backslash\text{to}\backslash)\sim$ -6V

<i>unused</i>		<i>stave0</i>	
31	2	1	0
-		0x0	

Reset