pCT Readout Electronics

Progress Report

Ola S. Grøttvik

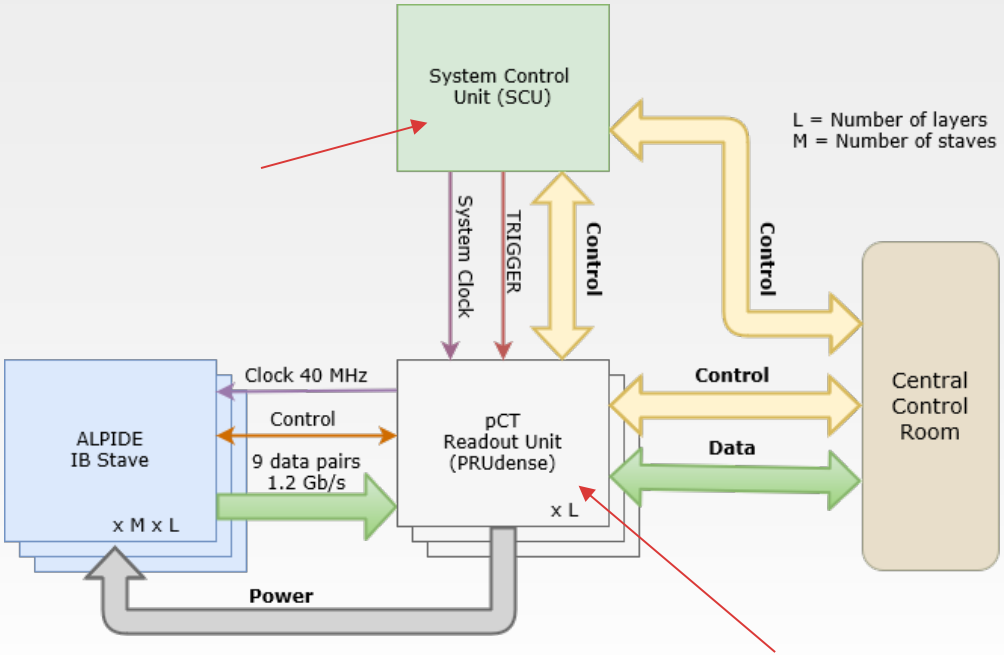
September 15th 2017

UNIVERSITY OF BERGEN

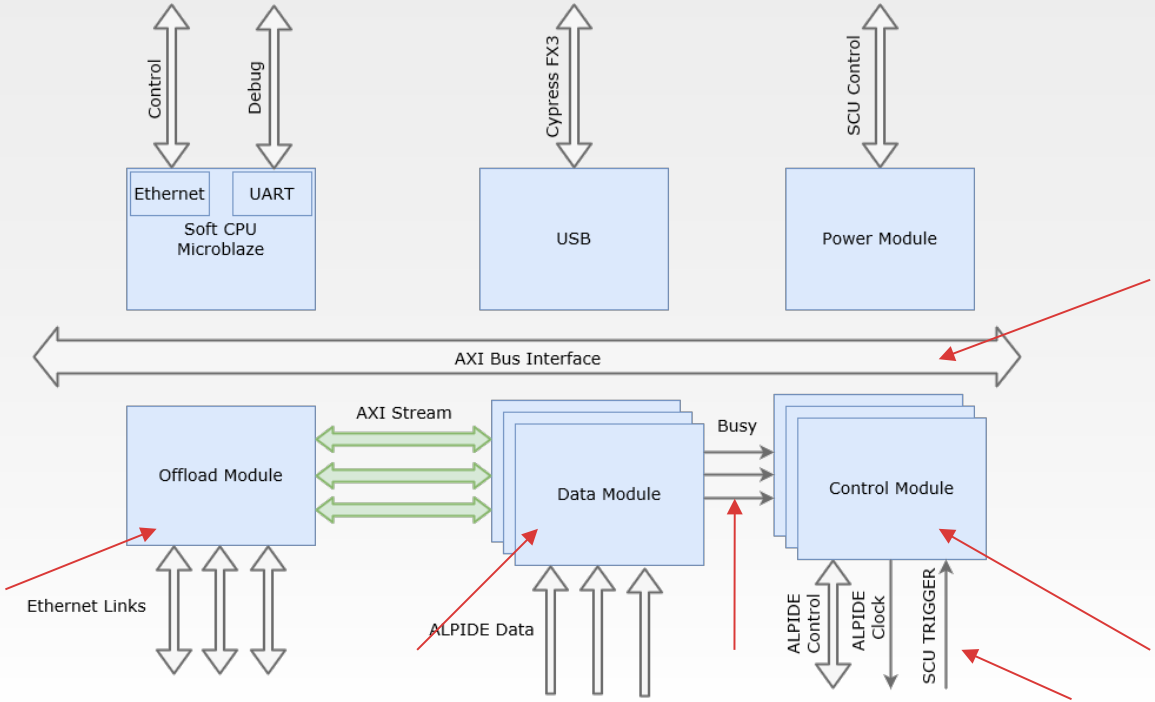
pCT Readout Requirements

- 1 RU for each layer, 1 state-of-the-art FPGA
- RU will interface up to 162(?) ALPIDE chips
- 1.2 Gb/s data streams
  - Sample, align, decode, filter, tag, buffer, combine, offload
- Control communication channel
  - Distribute TRIGGER command
- Provide clock and power
  - Monitor power usage
- Distance: 1-2 m between detector chip and RU

pCT Readout System Overview



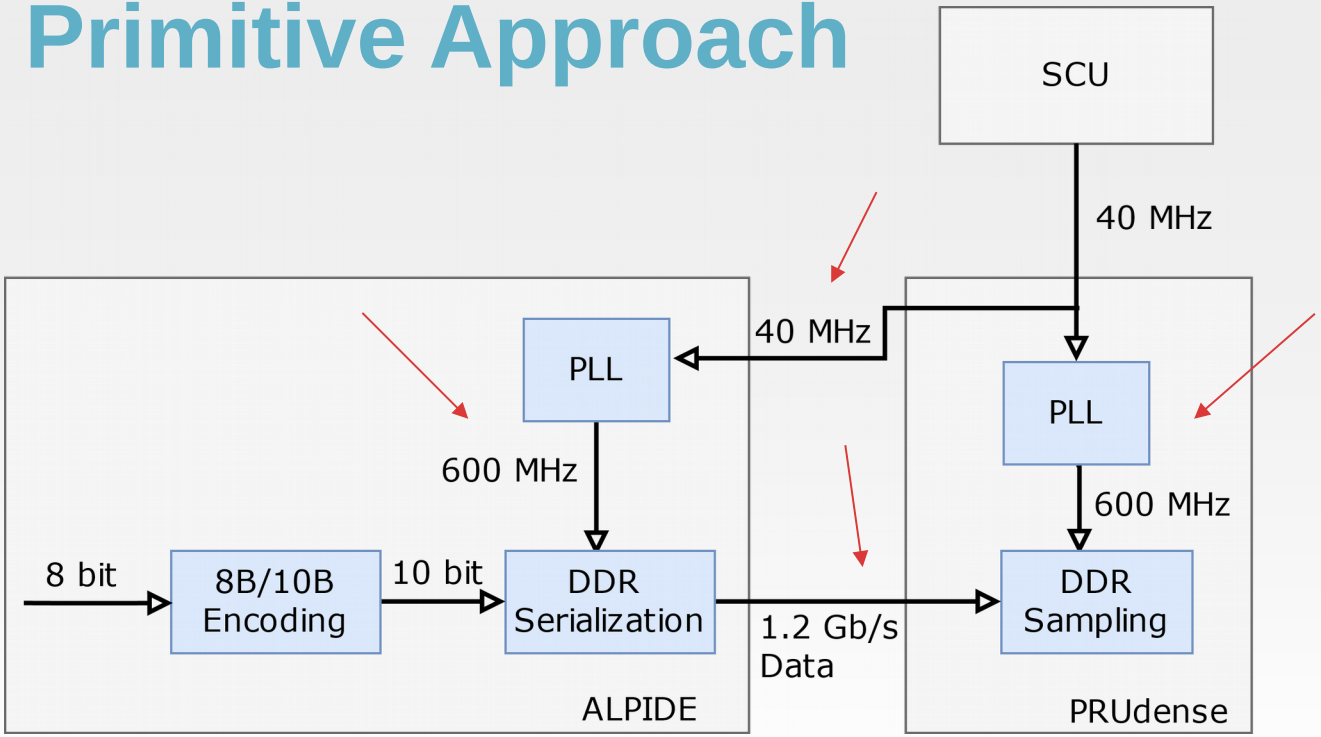
PRUdense Overview



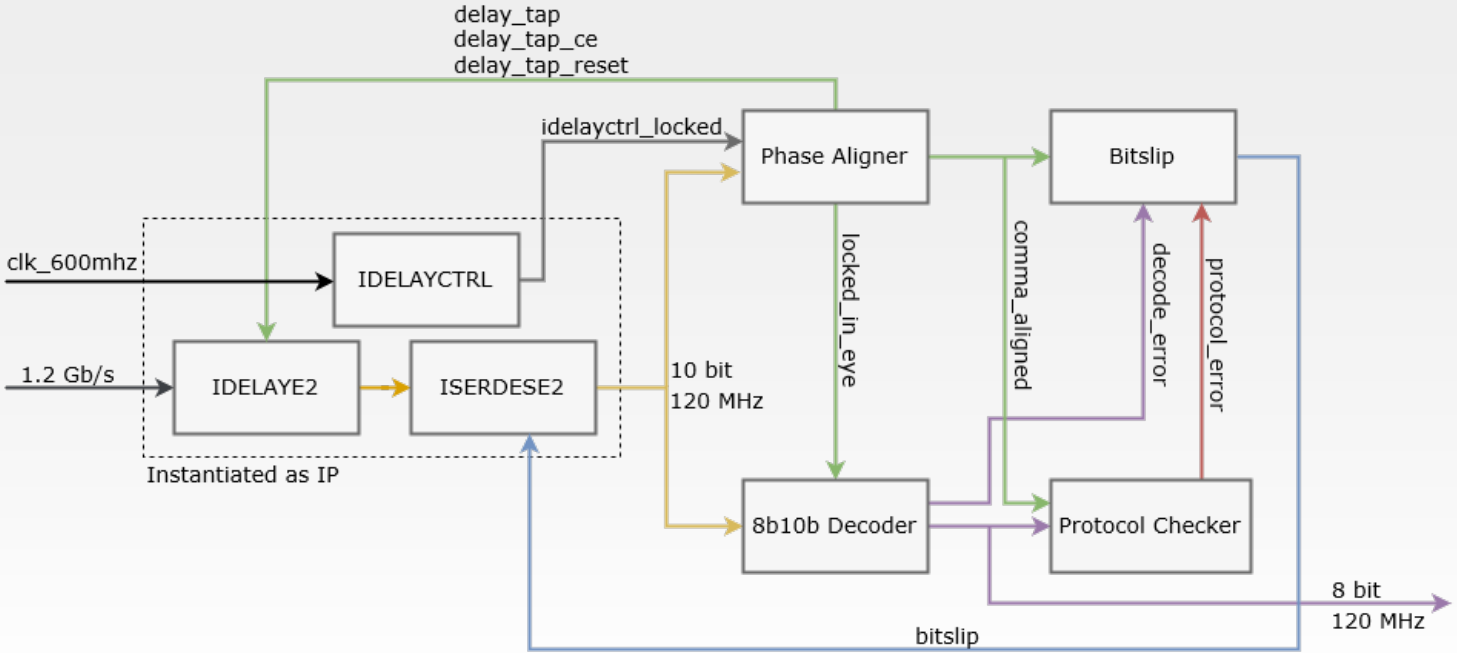
Clock and Data Recovery Design Implementations

- Existing design (ITS): Transceiver with fabric modules
- New design: Transceiver Only
- New design: Regular I/O Primitive Approach

I/O Primitive Approach



New Design: Automatic Phase and Word Alignment

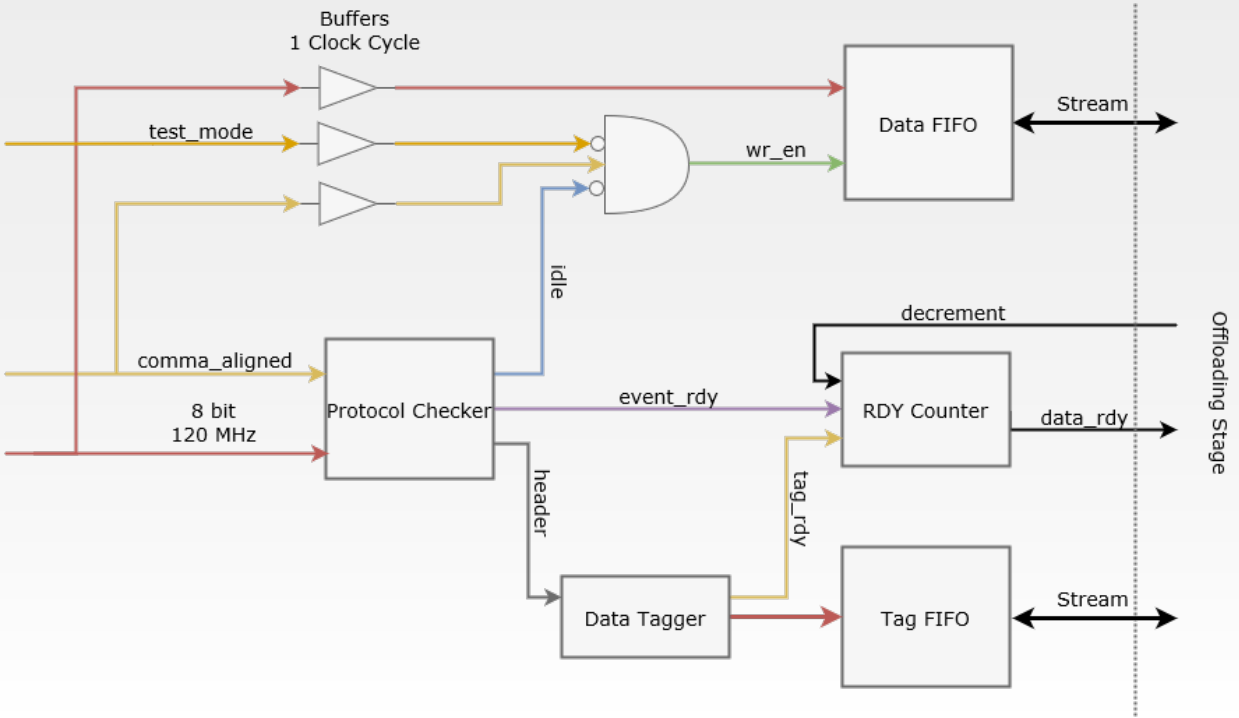


Test Results: Automatic Phase Alignment

	Test 1	Test 2	Test 3	Test 4	Test 5	Test 6
Test runs	1000	10	1000	10	1000	10
Length of each test (s)	60	21 600	60	21 600	60	21 600
Total time (s)	60 000	216 000	60 000	216 000	60 000	216 000
Cable length (m)	0.3	0.3	1.0	1.0	2.0	2.0
Temperature	Not supervised	Not supervised	Not supervised	Not supervised	Not supervised	Not supervised
Correct words	7.2×10^{12}	25.9×10^{12}	7.2×10^{12}	25.9×10^{12}	7.2×10^{12}	25.9×10^{12}
Incorrect words	0	0	0	0	**8306**	0
Runs with errors	0	0	0	0	[illegible]	0
Bitslips	9000[a]	82[a]	9059[a]	12[a]	1000[b]	10[a]
BER [c]	$< 13.0 \times 10^{-15}$	$< 3.9 \times 10^{-15}$	$< 13.0 \times 10^{-15}$	$< 3.9 \times 10^{-15}$	1.2×10^{-11}	$< 3.9 \times 10^{-15}$

[a] All bitslips occurred during word alignment and do not indicate an error.
[b] The connection between protocol checker and bitslip module is removed since it produced a lot more errors.
[c] Since the check is done on words, not bits; it is assumed that each incorrect word consists of a single bit error.

Filtering, tagging and buffering



Future work

- Upgrade the FPGA to new family => Increases I/O bandwidth
- Scale up design and investigate FPGA resource usage
- Radiation testing of I/O primitive approach => will triggering cause further errors?
- Determine final data protocol from PRUdense
- Complete filtering, tagging and buffering stage => determine buffer sizes
- Implement Processing System
  - Embedded software development
- Develop combining stage + offloading (Ethernet, GBTx, ?)
- Define and design SCU/DCS
  - Currently master project
- Design the PRUdense and SCU PCBs

UNIVERSITY OF BERGEN

Eco-Lighthouse®