global_regs

Version: 1.1

Thursday 5th November, 2020 14:33

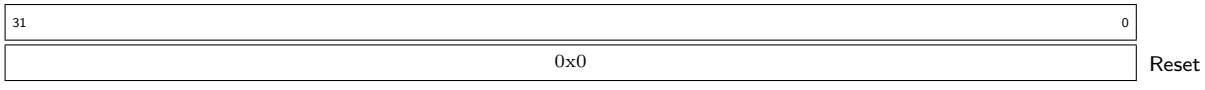
Global registers for version checks and basic system control.

1 Register List

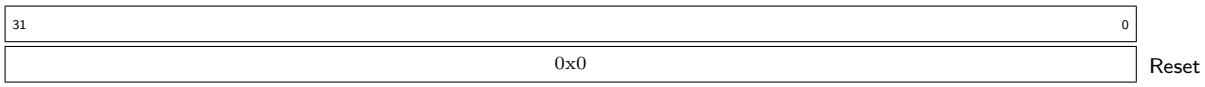
#	Name	Mode	Address	Type	Length	Reset
0	date_code	RO	0x00000000	DEFAULT	32	0x0
1	hash_code	RO	0x00000001	DEFAULT	32	0x0
2	led_blinky	RW	0x00000002	SL	1	0x1
3	reset_banks	RW	0x00000003	SL	1	0x0
4	enable_alpide_clock	RW	0x00000004	SL	1	0x0
5	ru_id	RO	0x00000005	SLV	6	0x0
6	max_size	RW	0x00000006	SLV	24	0x100000
7	max_wait_time	RW	0x00000007	SLV	16	0x258
8	filter_data_word	RW	0x00000008	FIELDS	2	0x3
9	empty_frame_compression	RW	0x00000009	SLV	16	0xFFFF
10	check_id	RW	0x0000000A	SL	1	0x1
11	DPA_delta	RW	0x0000000B	SLV	7	0x8
12	taps	RW	0x0000000C	SLV	9	0x0
13	system_clock_sel	RW	0x0000000D	SL	1	0x0
14	system_clock_input_status	RO	0x0000000E	SL	1	0x0
15	system_clock_drive_output	RW	0x0000000F	SL	1	0x0

2 Registers

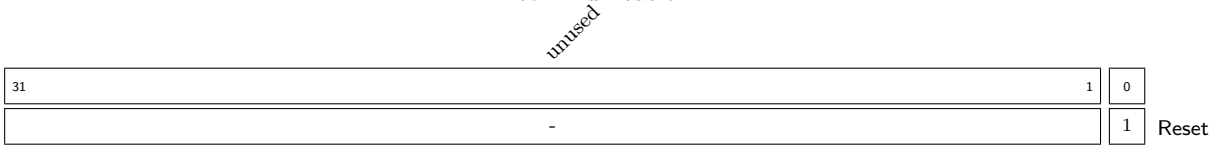
Register 2.1: DATE_CODE - RO (0x00000000)
The time of Vivado-project creation: 2-digit year, 2-digit month, 2-digit day, 2-digit hour.



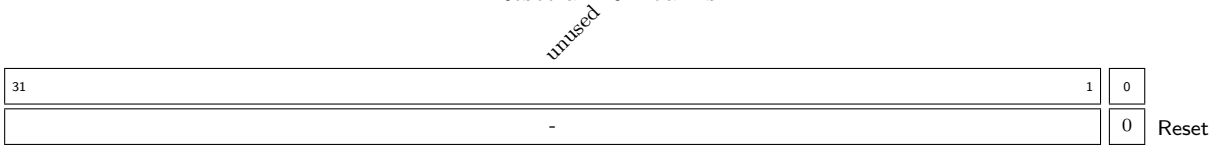
Register 2.2: HASH_CODE - RO (0x00000001)
Hash of commit-version used to build Vivado-project.



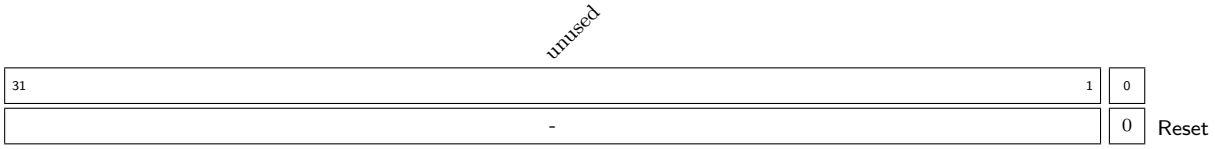
Register 2.3: LED_BLINKY - RW (0x00000002)
Enables blinking of LEDs that confirm successful FPGA programming. Can be turned off to confirm AXI communication.



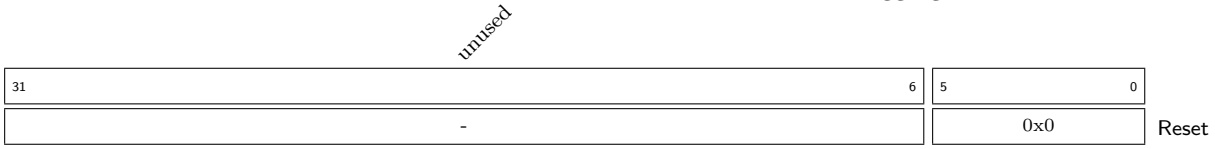
Register 2.4: RESET_BANKS - RW (0x00000003)
Reset all RX banks.



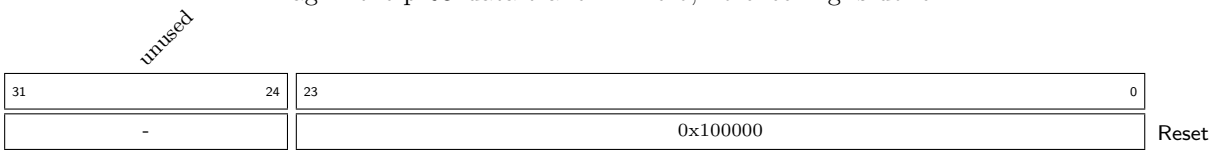
Register 2.5: ENABLE_ALPIDE_CLOCK - RW (0x00000004)
Enables the 40 MHz clock output to all ALPIDE staves connected to RU.



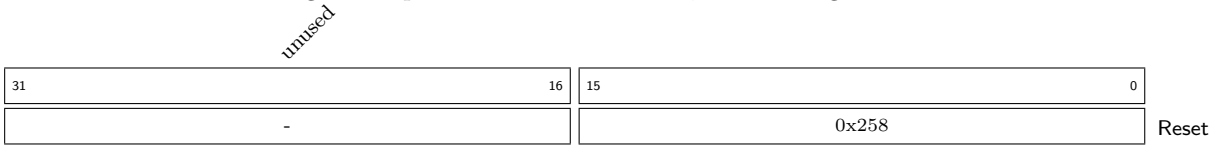
Register 2.6: RU_ID - RO (0x00000005)
Readout Unit identification number. Used in data tagging.



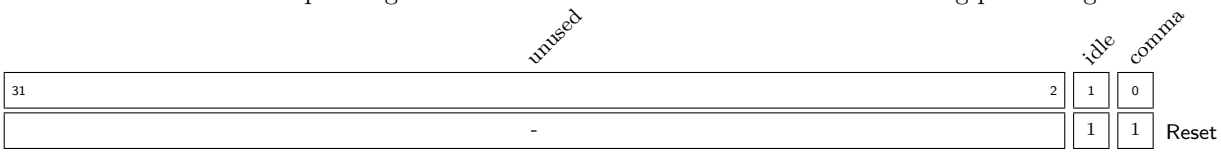
Register 2.7: MAX_SIZE - RW (0x00000006)
The maximum size of an frame. If the frame is larger than this number, a fatal frame error is triggered, and the processing of the frame is aborted. This error is marked with the Frame Error + Max Size Error flag in the pRU data trailer. If zero, no checking is done.



Register 2.8: MAX_WAIT_TIME - RW (0x00000007)
The maximum time, measured in clock cycles (120 MHz), to wait for a valid word during processing of an frame. If the wait time is larger than this amount of clock cycles, a fatal frame error is triggered, and the processing of the frame is aborted. This error is marked with the Frame Error + Max Wait Time Error flag in the pRU data trailer. If zero, no checking is done.



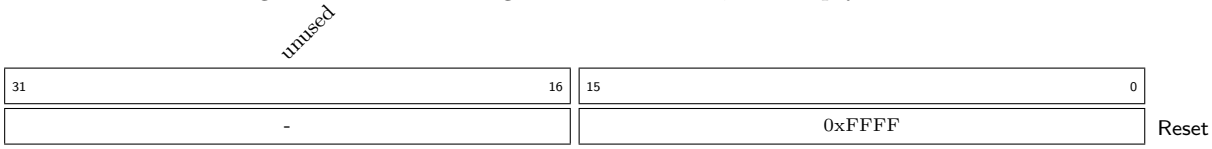
Register 2.9: FILTER_DATA_WORD - RW (0x00000008)
Decides wether the corresponding word should be filtered out of the stream during processing an frame.



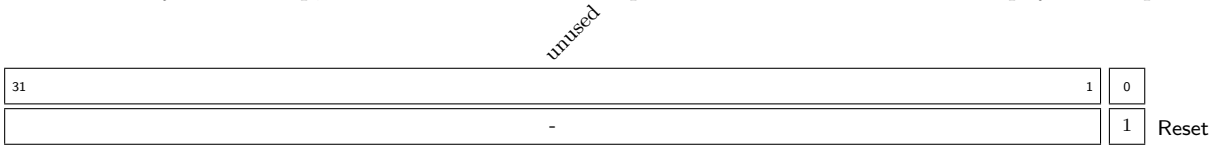
comma Filter out 0xBC control words. Requires that the 8b10b decoder also determines as a control character.

idle Filter out 0xFF.

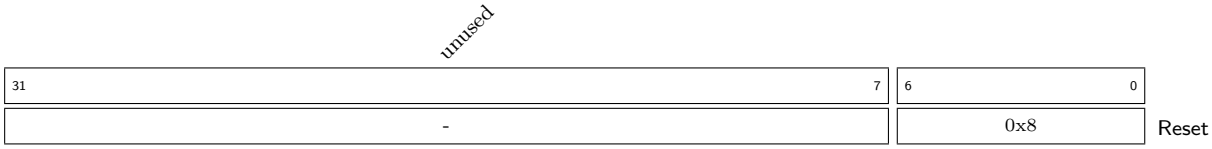
Register 2.10: EMPTY_FRAME_COMPRESSION - RW (0x00000009)
Compress the number of pRU Empty Words transmitted. The value determines how many CONSECUTIVE empty frames required before transmitting a pRU Empty Word. Empty frames that are not in a consecutive sequence that have at least this many frames, will be dropped with no other action than incrementing frame ID. If this register is set to zero, NO empty frame words are written.



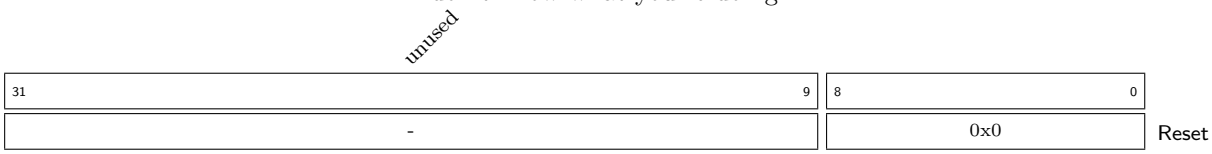
Register 2.11: CHECK_ID - RW (0x0000000A)
When asserted, protocol checker will require that the ALPIDE header has the correct chip ID before starting a frame. This may prevent some fake frames under jitter-circumstances right before an actual frame is ready on the chip, and also assures that the pRU data will match the actual physical chip ID.



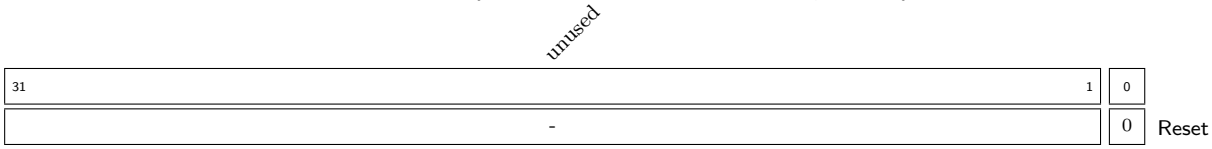
Register 2.12: DPA_DELTA - RW (0x0000000B)
The amount the DPA logic increments or decrements the line delay (in taps) in every adjustment operation. WARNING: Larger than 8 might cause glitches in RX_BITSLICE primitives. Do not change if you do not know what you're doing!



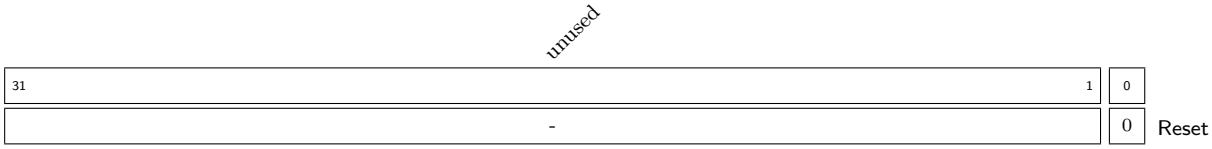
Register 2.13: TAPS - RW (0x0000000C)
If not zero, force a number of bitslice delay taps to yield a half unit interval. Should never be used if you don't know what you're doing!



Register 2.14: SYSTEM_CLOCK_SEL - RW (0x0000000D)
Select between local and system clock. 0 -> local clock, 1 -> system clock.



Register 2.15: SYSTEM_CLOCK_INPUT_STATUS - RO (0x0000000E)
System clock status. Indicates whether MMCM acheives lock.



Register 2.16: SYSTEM_CLOCK_DRIVE_OUTPUT - RW (0x0000000F)
Assert to drive the BTBI clock from this FPGA.