9-chip String Simulation - and proposed 9-chip string redesign

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1 Introduction

The following simulations are performed with Hyperlynx 9.4.2. The goal of the simulations is to identify transmission line problems with the current 9-chip string design and propose another solution. Note that these simulations do not aim to identify problems with the power connections and the subsequent jitter issues experienced in hardware. It should also be noted that these simulations likely represent a best case scenario, as only part of the environment is included in the stack-ups. Therefore, they should be used for "what-happens-if" tests rather than be taken as accurate models.

In the last section we propose a solution for the layout of the redesigned 9-chip string card.

2 Baseline Simulation

To ensure realistic driver and buffer attributes, the IBIS model for the Texas Instruments LVDS Buffer IC DS15MB200 is used for both as TX and RX. The eye diagram mask is set according to Xilinx HP IO pin LVDS specifications with a minimum differential voltage of +/- 100 mV. The stimulus is always a 1.2 Gb/s PRBS-7 sequence which is repeated 50 times. The eye diagram is measured over the 100 ohm termination resistor.

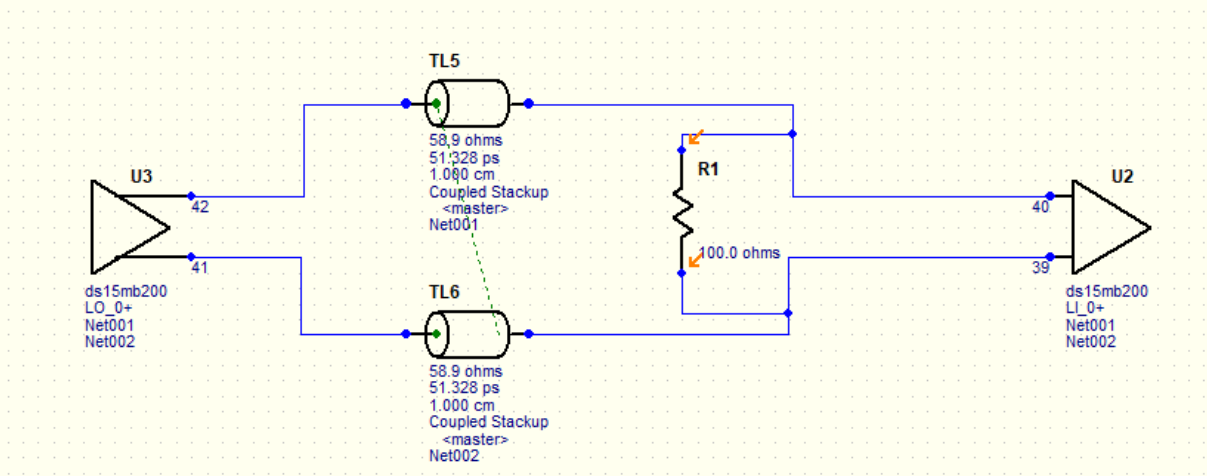

Figure 1: Ideal Transmission Line with Driver and Receiver

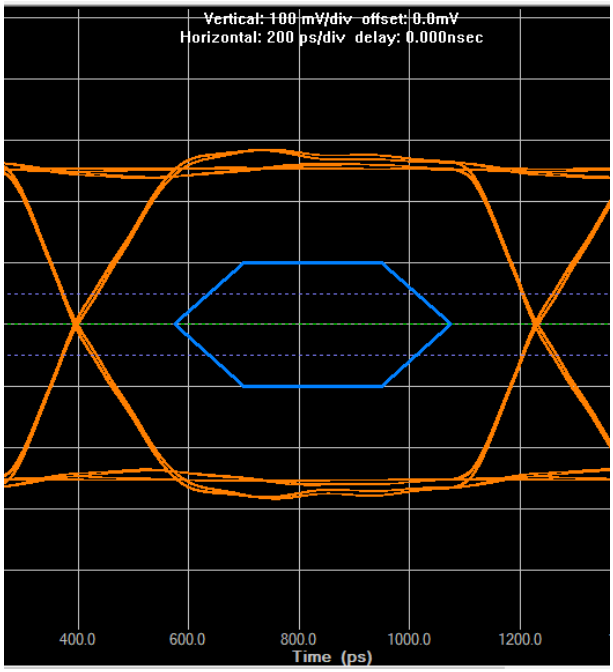

Figure 2: Ideal Transmission Eye Diagram - Eye Width: 437 ps, Eye Height: 486 mV

3 Current Design

The simulation for the current design consists of 5 parts:

1. Chip Cable trace (including extra stubs)
2. Flex Cable trace (9 chip string) on the absorber
3. Flex Cable trace outside the absorber
4. FPC to Firefly Transaction Card
5. Firefly cable mimic

However, although a lot has been done to mimic reality, the simulation results and the actual measured results may differ significantly. E.g. no connector models are included, and the Firefly cable might introduce some more attenuation in real life (although negligible reflection). See A on page 13 for a note about Firefly.

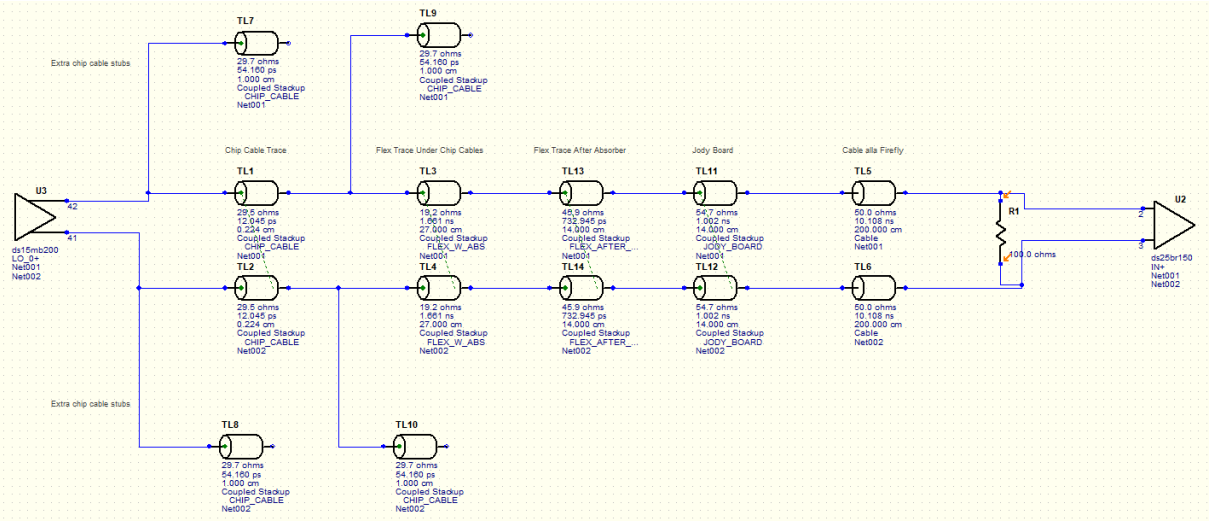

Figure 3: Current Design

3.1 Chip Cable on ALPIDE

The chip cable part of the simulation is completed by adding reference half planes on either side of the differentially coupled transmission lines. This mimics the DVSS ground plane on the chip cable. With a trace width and trace separation of 100 µm, the calculated Zdiff is 56 ohm.

Table 1: Chip Cable Stackup Properties

Layer	Type	Usage	Thickness (µm)	Er	Metal	Loss Tangent
CHIP_CABLE_AL	Metal	Signal	30		Aluminum	
CHIP_CABLE_PI	Dielectric	Flex Substrate	20	3.4		0.02
EPOXY	Dielectric	Adhesive	3	3.4		0.02
ALPIDE	Metal	Plane	100		Copper	
EPOXY	Dielectric	Adhesive	5	3.4		0.02
ABSORBER	Metal	Plane	100		Aluminum	

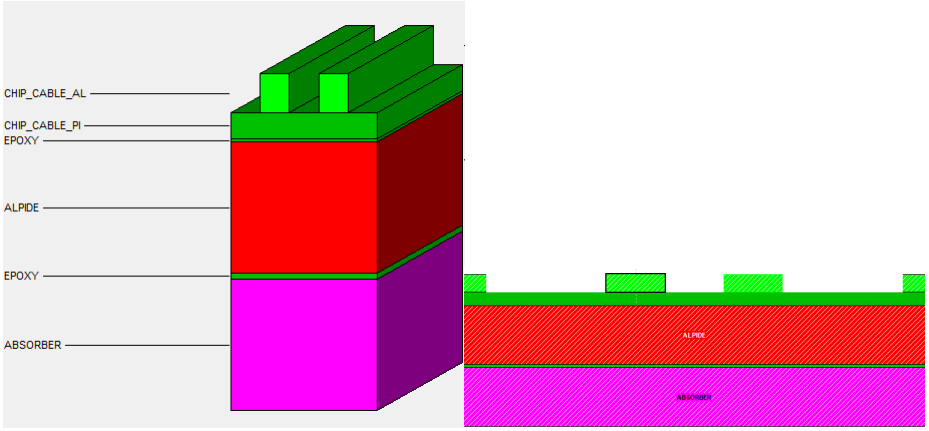

Figure 4: Chip Cable Stackup

3.2 Flex Cable On Absorber

For the flex cable trace on the absorber we need to consider both the absorber itself, but also the chip cables on top of the trace. As most of the chip cable is a ground plane, we need to model it as such.

Hence, with a trace width and trace separation of 100 µm the calculated Zdiff is only 44.7 ohm. The modeling of the chip cable as a plane has a damaging effect on the eye diagram because the dielectric thickness to nearest plane is so thin. If we model the chip cable as a signal layer, the Zdiff jumps to 72.5 ohm.

Table 2: Flex Cable On Absorber Stackup Properties

Layer	Type	Usage	Thickness (µm)	Er	Metal	Loss Tangent
CHIP_CABLE_AL	Metal	Plane	30		Aluminum	
CHIP_CABLE_PI	Dielectric	Flex Substrate	20	3.4		0.02
EPOXY	Dielectric	Adhesive	8	3.4		0.02
TOP_LAYER_AL	Metal	Signal	30		Aluminum	
TOP_LAYER_PI	Dielectric	Adhesive	20	3.4		0.02
EPOXY	Dielectric	Adhesive	5	3.4		0.02
BOTTOM_LAYER_PI	Dielectric	Flex Substrate	20	3.4		0.02
BOTTOM_LAYER_AL	Metal	Plane	30		Aluminum	
EPOXY	Dielectric	Adhesive	5	3.4		0.02
SMD_FLEX_PI	Dielectric	Flex Substrate	20	3.4		0.02
SMD_FLEX_AL	Metal	Signal	30		Aluminum	
EPOXY	Dielectric	Adhesive	5	3.4		0.02
KAPTON_COVER	Dielectric	Cover Layer	40	3.4		0.02
EPOXY	Dielectric	Adhesive	5	3.4		0.02
ABSORBER	Metal	Plane	100		Aluminum	

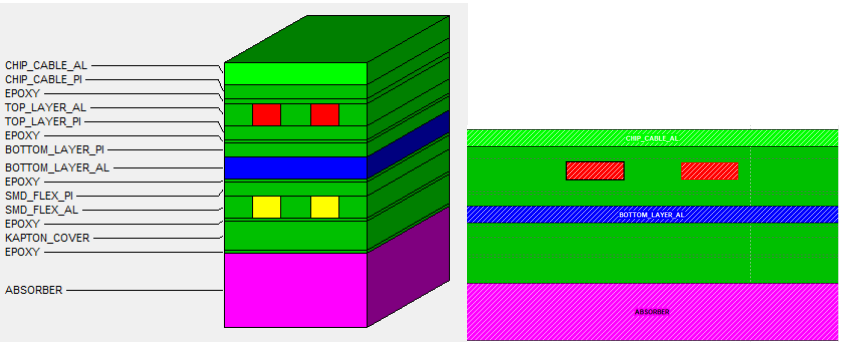

Figure 5: Flex Cable On Absorber Stackup

3.3 Flex Cable Outside Absorber

The flex cable outside of the absorber is much simpler to model as there are only two layers. There is one ground layer directly under the differential pairs, hence it is modeled as a microstrip design. With a trace width and trace separation of 100 µm the calculated Zdiff is 83.5.

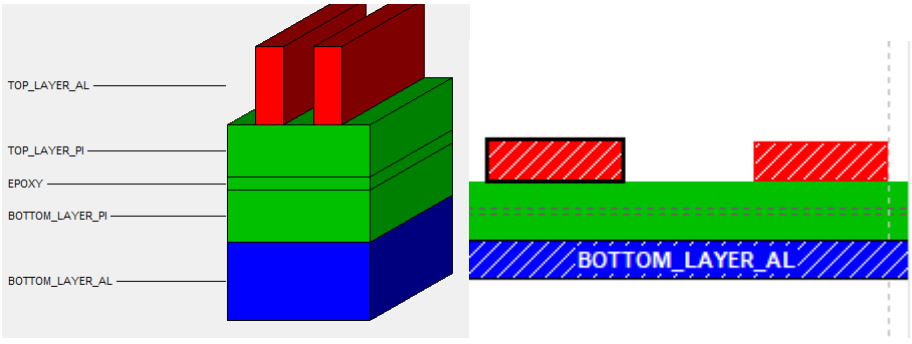

Figure 6: Flex Cable Outside Absorber Stackup

3.4 Transition Card

The transition card stack-up is exact copy of Jody's design. The calculated Zdiff based on arbitrarily chosen differential signal in the PCB layout is 94.4 ohm.

3.5 Simulation Results

The simulated eye diagram does not reach desired values (see figure for values). The eye diagram simulation matches the actual measured value for the 9-chip string in hardware, where the ALPIDE is driving with a maximum strength and maximum pre-emphasis. If we model the chip cable as a signal layer, the eye diagram is somewhat better, but still not within comfortable levels with an eye width of 396 ps and eye height of 172 mv.

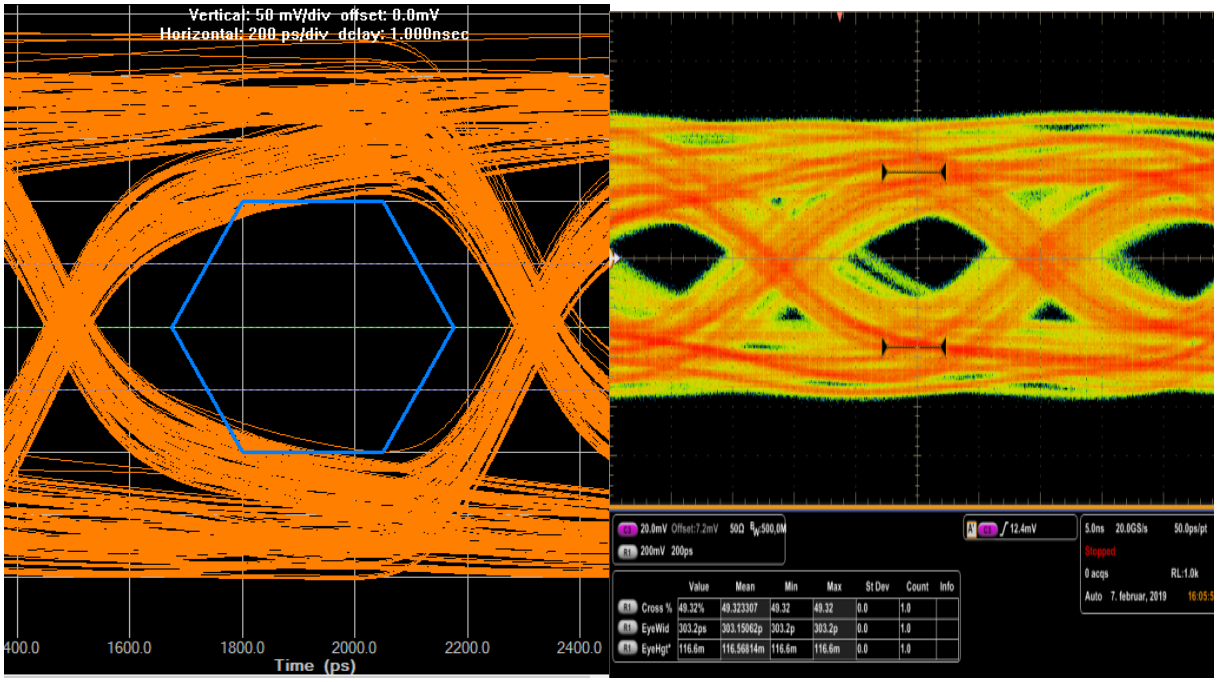

Figure 7: Left: Simulated Current Design Eye Diagram - Eye Width: 308 ps, Eye Height @ 50% UI: 104 mV. Actual measured eye diagram with maximum drive strength and pre-emphasis.

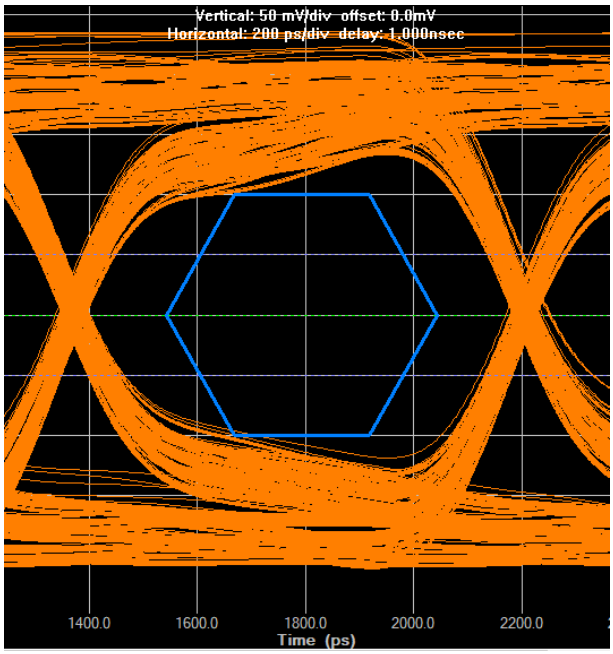

Figure 8: Current Design Eye Diagram - Chip Cable as signal layer - Eye Width: 396 ps, Eye Height @ 50% UI: 172 mV

The length of the trace outside of the absorber does also negatively impact the eye diagram.

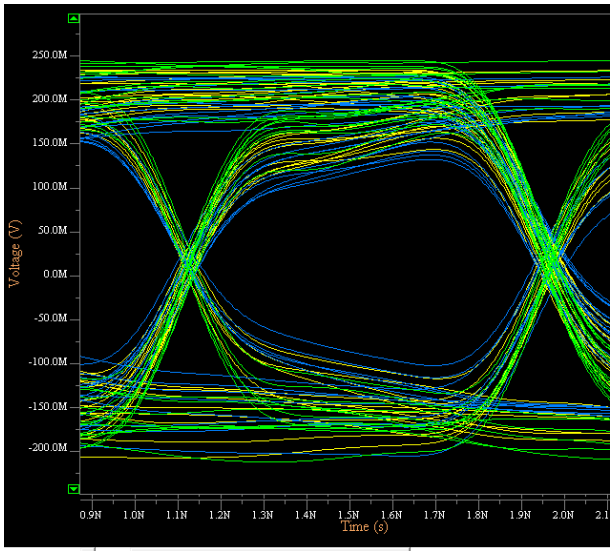

Figure 9: Sweep of length for trace outside absorber: Green 1 cm, Yellow: 14 cm, Blue: 30 cm.

The chip cable stubs is the source of some reflection, so reducing the stub lengths reduces reflections resulting in better eye height.

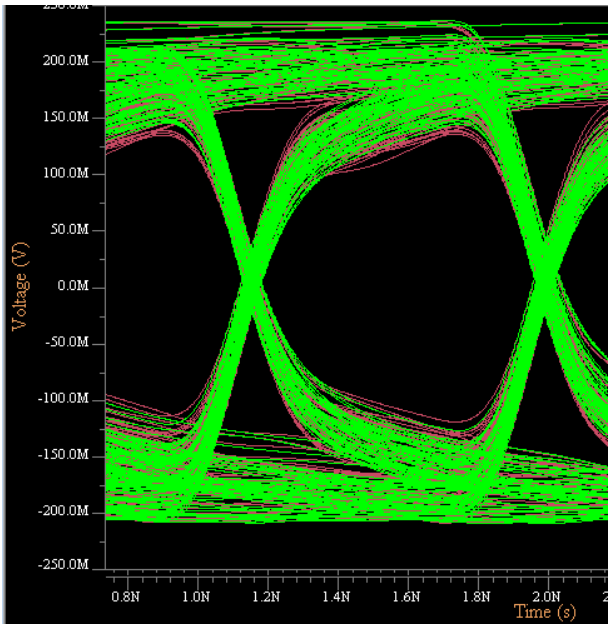

Figure 10: Comparison of chip cable stub lengths: Green: 0.01 cm, Red: 1 cm.

4 Proposed redesign

From the simulations we think the problem with the present design is a combination of transmission loss, which is dominated by electrical attenuation, and distortion due to differential impedance mismatch between the design parts. In a lossy transmission line the resistance per length increases with the square root of the frequency, due to skin depth, and the shunt conductance per length increases linearly with frequency due to the dissipation factor of the dielectric, ref. for example [1]. The RF sheet resistance for a single-metal system is calculated as:

$$R_{RFSH} = \sqrt{\frac{\pi \mu_0 \mu_R}{\sigma}}$$

Sigma is the metal's conductivity in Siemens/meter; sigma is 1/rho, where rho is resistivity and is in units of ohm-meters. RF sheet resistance units are ohm/square.

Using this simple equation we find that the RF sheet resistance is 0.0112 ohm/square, and that a 300 mm long wire with 0.1 mm width has a RF resistance of 44.8 ohm at 1.2 GHz, resulting in 1.7 dB loss just from conductor loss.

$$\alpha_{cond} = 10 \log(e) \frac{R_{RFSH}}{Z_0}$$

This equation is valid for single ended signals, but the differential impedance is, to the first order, 2 times Z_0.

From the conductive loss equation we see that the loss can be reduced by decreasing the R_{RF}/Z_0 ratio, but we also want to keep the characteristic differential impedance as close as possible to 100 ohm.

We propose a new stack-up for the flex trace as shown in 11. The main purpose is to improve the impedance matching while keeping the conductive losses low. Here all the LVDS pairs are on the left side, and power planes and routing is on the right hand side. The dielectric insulation towards the absorber and the chip cable should be as thick as possible, preferably in the more than 100 µm upwards and downwards. Also, by adjusting the trace thicknesses and separation to 90 and 120 µm respectively, we achieve a Z_{diff} of 87 ohm. A significant improvement from the current design.

In the simulation of this design, one of the chip cable stubs are removed, as it is not required. Also, the trace after the absorber has been reduced to 3 cm since we need to minimize the total length of the the flex card due to its losses.

~ 5 mm	Under abs: ~ 5 mm, Outside: ~10 mm		
Dielectric	Power Lines (Al)	30 µm	
Dielectric	Dielectric	20 µm	
Dielectric Epoxy	Dielectric Epoxy	5 µm	
Dielectric	Dielectric	20 µm	
Diff Signals (Al)	Power Lines (Al)	30 µm	DVSS Only
Dielectric Epoxy	Dielectric Epoxy	5 µm	
Dielectric	Dielectric	20 µm	
Dielectric	Power Lines (Al)	30 µm	

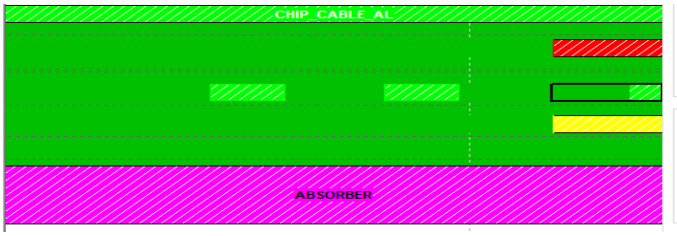

Figure 11: Proposed Flex Trace Design

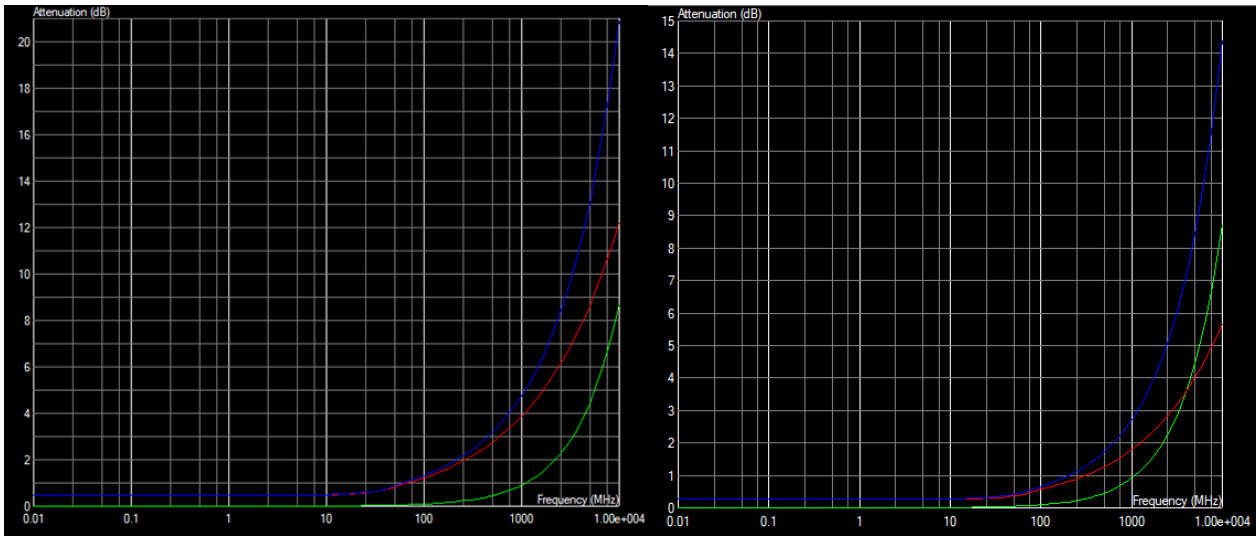

Figure 12: Comparison of attenuation for the flex trace over the chip cables, current design to the left and proposed new design to the right. Green curve shows dielectric attenuation, red is conductive attenuation and blue is total attenuation.

As one can see from the eye diagram, the results are significantly better.

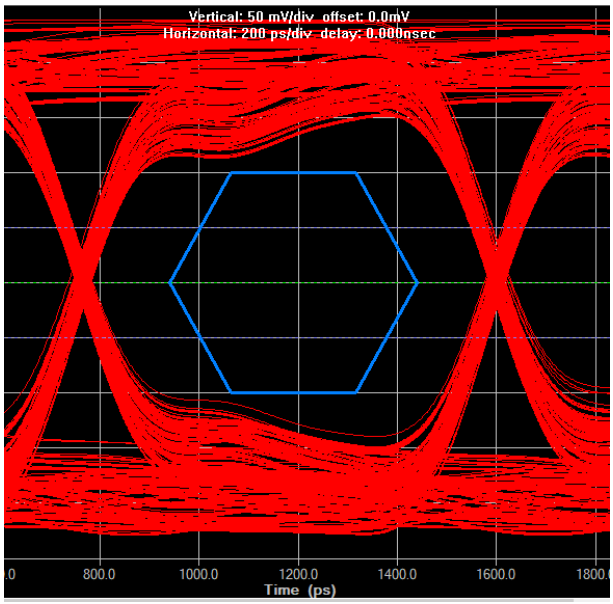

Figure 13: Proposed Design Eye Diagram - Eye Width: 416 ps, Eye Height @ 50% UI: 208 mV

5 Crosstalk

In order to evaluate if there is a need to shield the differential pairs with ground lines in between them, a crosstalk simulation has been performed on the flex card, including the flex trace on absorber and after the absorber. Two differential transmission lines are coupled together on both stack-ups with a distance of 150 µm apart. The victim transmission line is not driven, but is pulled low in its inputs.

The cross talk is larger in the proposed design than in the present design, mainly because the ground planes are further away from the signal traces. From the simulation results below we see that the victim pair sees 12 mV p-p cross talk, which probably will be tolerable if the signal level is improved due to the proposed design change. Larger pair-to-pair distances is favorable in order to minimize crosstalk.

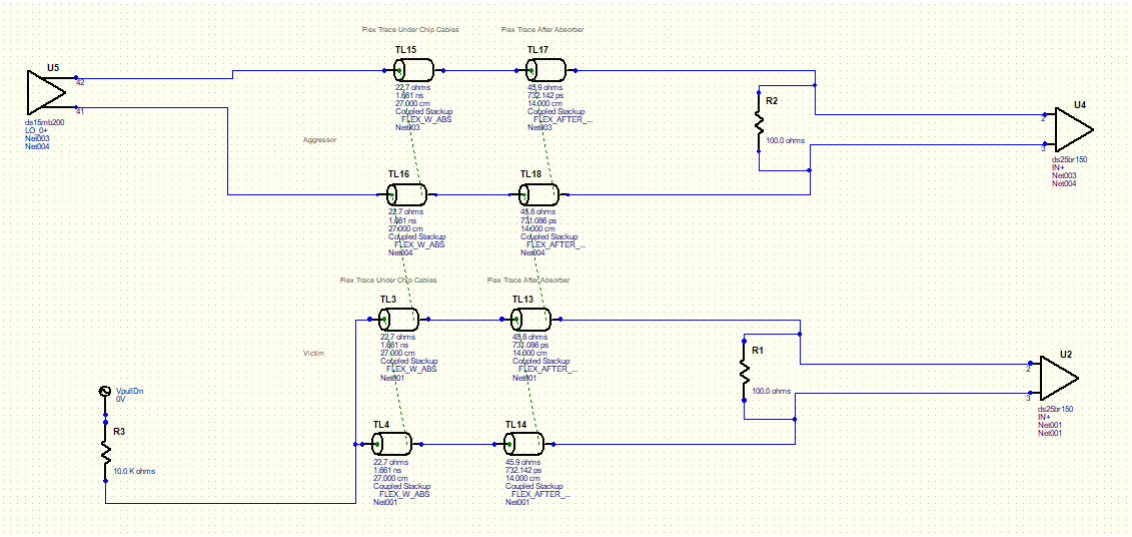

Figure 14: Crosstalk Simulation Setup

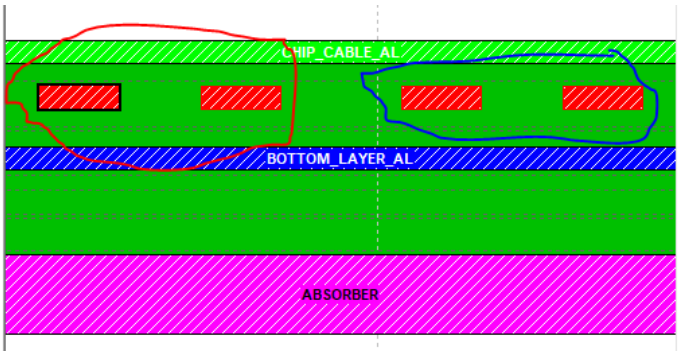

Figure 15: Current design crosstalk simulation: red: aggressor, blue: victim.

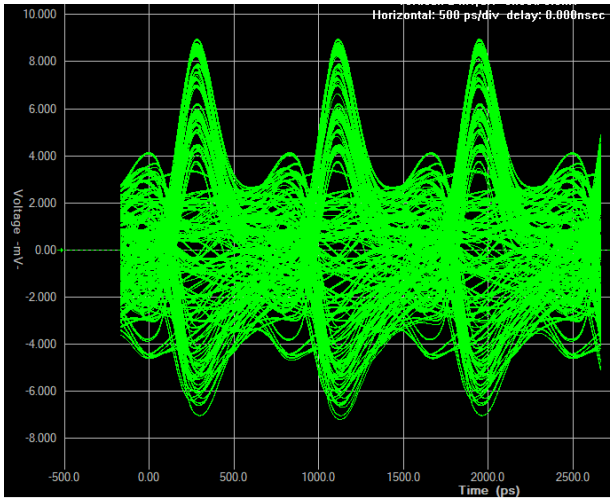

Figure 16: Current design crosstalk on victim from a 1.2 Gb/s PRBS aggressor.

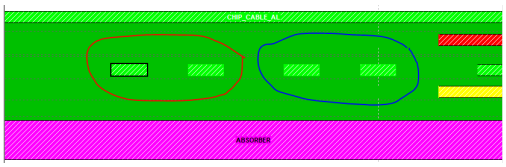

Figure 17: Proposed design crosstalk simulation: red: aggressor, blue: victim.

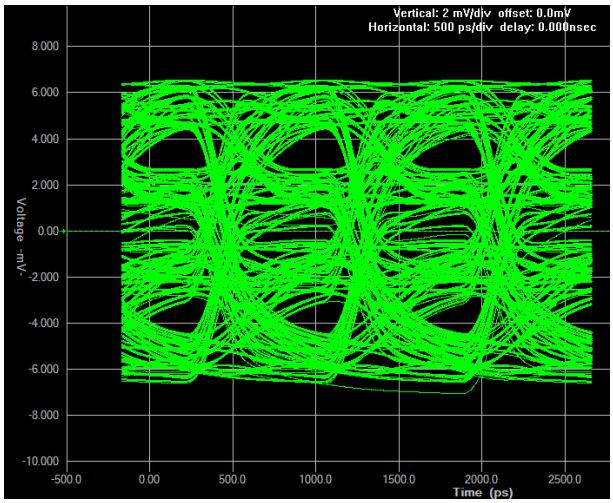

Figure 18: Proposed design crosstalk on victim from a 1.2 Gb/s PRBS aggressor. Aggressor on left side.

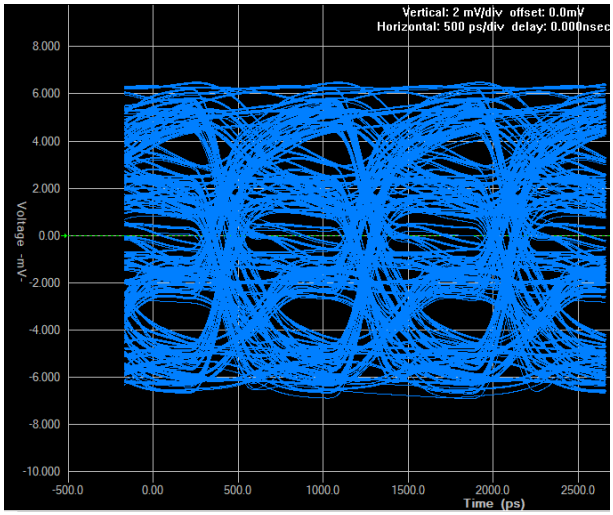

Figure 19: Proposed design crosstalk on victim from a 1.2 Gb/s PRBS aggressor. Aggressor on right side.

6 Proposed Layout Change

Since we need to avoid routing and planes above and below the high speed lines we propose to use 3 layers for power connections. In addition, we need to split DVDD and PVDD from the zip-connector side in order to minimize DVDD noise on the PVDD pad of the ALPIDEs. We should also discuss the position of the decoupling capacitors. If we could place them on top of the ALPIDE, .i.e. on the chip cable it would be the best solution from decoupling perspective. This also reduces heigth compatability problem between the ALPIDD

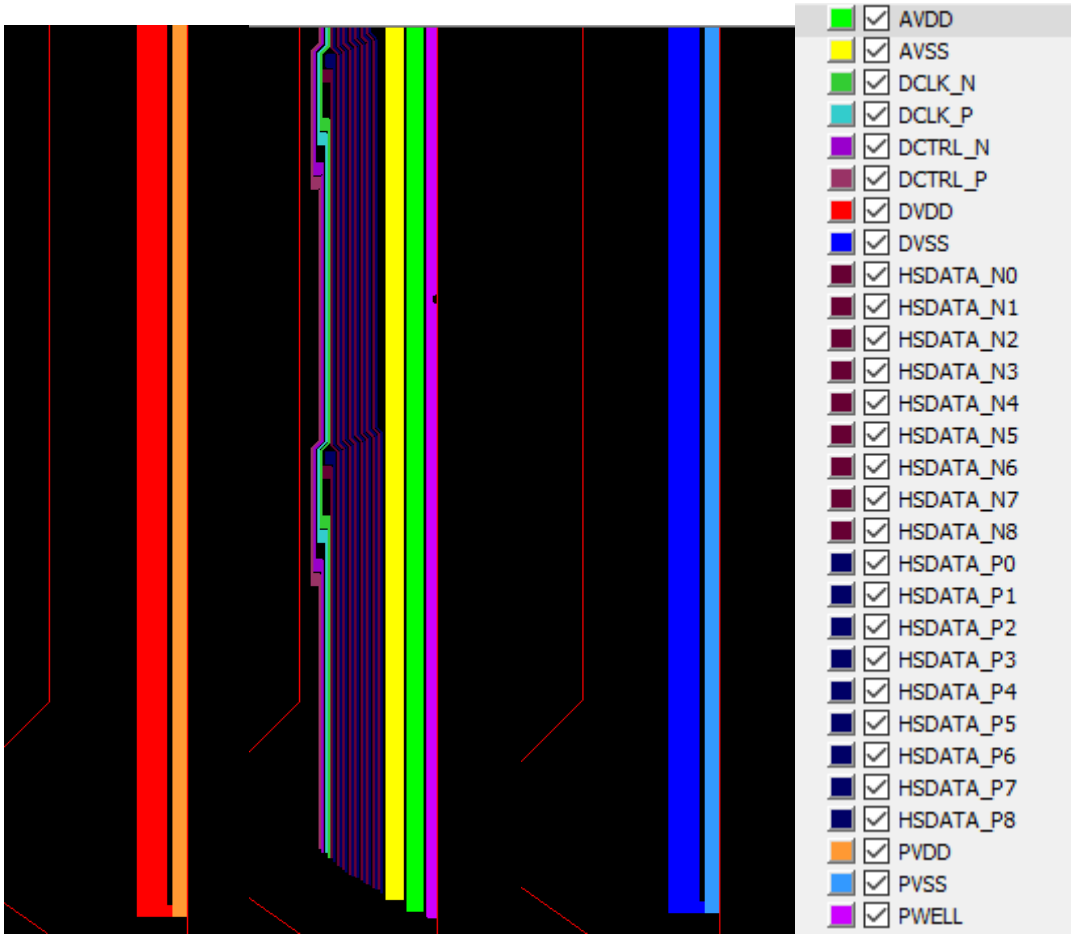

Figure 20: Proposed design layout, layer 1 to the left followed by layer 2 and 3 and signal legend.

6.1 Summary of proposed changes

1. Avoid routing and planes above the high speed link
   (a) Modify assembly procedure/gluing/etc in order to accommodate thicker dielectric above and below high speed wires (stripline design).
2. Short connection to decouple C
   (a) Use A pads or
   (b) Place capacitor flex on top of chipcable?
3. Split PVDD and DVDD from zip-connector side
4. Fix HDATA N/P swap
5. Skip ALPIDE ID 7, i.e. use ID 0-6 and 8-9
6. Remove one of the chip cable stubs

A Appendix: Firefly

Although Samtec has not released s-parameters for the Firefly cable, some more effort was done to try to show the effects of the cable in simulation than what is shown above. Based on [2], a quasi-model was generated and tested with a 14 Gb/s PRBS-7 stimuli to obtain an eye diagram resembling the High Speed Characterization Report [3]. The eye diagram is shown below.

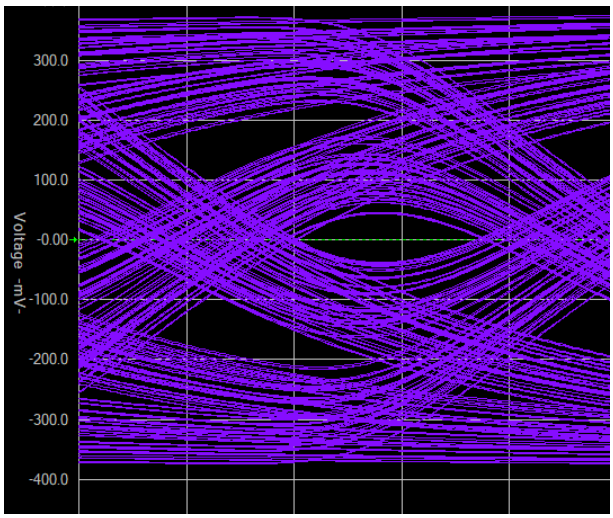

Figure 21: Model of 0.5m Firefly at 14 Gb/s PRBS-7.

With this model inserted in the simulation, we see, as expected, a significant attenuation for both designs. This further emphasizes the point that we should try to reduce loss-effects as best as we can earlier in the electronics chain.

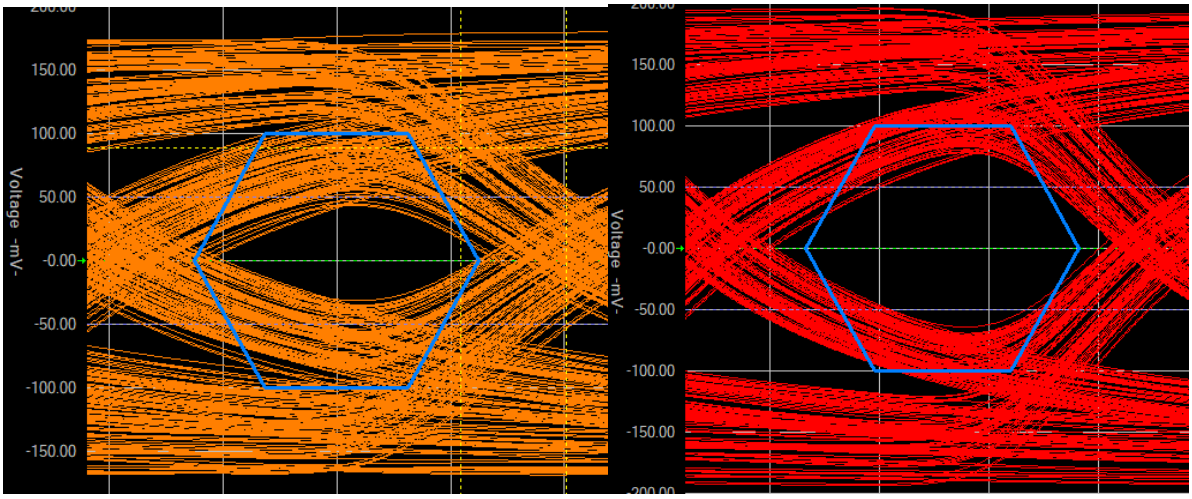

Figure 22: Simulation results with quasi-model of Firefly. Left: Current Design with Eye Height: 69 mV - Right: Proposed Design with Eye Height: 130 mV.

References

[1] Eric Bogatin, *Signal and power integrity - simplified*, Prentice Hall, 2010

[2] http://suddendocs.samtec.com/notesandwhitepapers/ttf-36100-xx-xx_datasheet.pdf

[3] http://suddendocs.samtec.com/testreports/hsc-report_ecue_web.pdf