trigger_manager

Version: 2.0

Monday 14^{th} December, 2020 20:10

The Trigger Manager is responsible for synchronization and trigger commands. It can be configured in standalone mode, or in a master/slave configuration with other pRUs. The module is either master or slave based on the physical settings of the pRU board. The Trigger Manager has direct access to the ALPIDE Control module, and can transmit the most common broadcast messages.

1 Register List

#	Name	Mode	Address	Type	Length	Reset
0	status	RO	0x00000000	FIELDS	5	0x3
1	config	RW	0x0000001	FIELDS	3	0x3
2	cmd	RW	0x0000002	FIELDS	15	0x0
3	msg	RW	0x0000003	SLV	8	0x0
4	arm_and_execute	PULSE	0x0000004	SL	1	0x0
5	btbi_master_status	RO	0x0000005	FIELDS	7	0x0
6	btbi_slave_status	RO	0x0000006	FIELDS	12	0x0
7	btbi_slave_cmd	RO	0x0000007	FIELDS	15	0x0
8	num_triggers	RW	0x0000008	DEFAULT	32	0x1
9	trigger_to_execution_delay	RW	0x0000009	DEFAULT	32	0x7
10	slave_trigger_to_execution_delay	RW	A0000000x0	DEFAULT	32	0x2
11	sequence_delay	RW	0x000000B	DEFAULT	32	0x28
12	pulse_trigger_delay	RW	0x000000C	DEFAULT	32	0x28
13	num_trains	RW	0x000000D	DEFAULT	32	0x1
14	trains_delay	RW	0x000000E	DEFAULT	32	0x28
15	trigger_source	RW	0x000000F	SLV	2	0x3
16	alpide_mode	RW	0x0000010	SLV	1	0x1
17	absolute_time	RO	0x0000011	DEFAULT	32	0x0
18	spill_id	RO	0x0000012	SLV	16	0x0
19	frame_id	RO	0x0000013	DEFAULT	32	0x0

2 Registers



Register 2.2: CONFIG - RW (0x00000001) Configuration of the module.

ent spillid Pock all chil standalone UIIIE 31 0 3 0 1 Reset -

standalone	When standalone, the Trigger Manager does not bother with BTBI com- munication.
lock_alp_ctrl	When standalone, the ALPIDE Control module must be locked manually with this register. Disregarding this might cause conflicts with the MM- interface access to the ALPIDE Control module.

 $increment_spill_id \quad {\rm Increment} \; {\rm Spill} \; {\rm ID} \; {\rm at} \; {\rm the} \; {\rm end} \; {\rm of} \; {\rm each} \; {\rm trigger} \; {\rm train}. \; {\rm NOT} \; {\rm IMPLEMENTED}.$



Register 2.3: CMD - RW (0x0000002) The command to be executed by master or standalone pRU.

Register 2.4: MSG - RW (0x00000003) The message to transfer to the pRU slaves	s.		
111110ed			
31 8	8	7 0	
-		0x0	Reset



-

31

Reset

0

Register 2.6: BTBL_MASTER_STATUS - RO (0x00000005) Status of the BTBI communication module when configured as master.



Reset

busy	Busy with slave communication.
waiting	Waiting for ack or unack.
all_ack	All slaves are acknowledging, i.e. no slaves are driving the ack signal down. Note that this signal is weakly driven by a weak pull-up resistor.
timeout	High when timeout occurred when waiting for ack.
$wait_for_lock$	Waiting for the ALPIDE Control module to lock.
$ready_for_trig$	We are ready to start triggering.
err	Something went wrong, e.g., ALPIDE Control didnt lock in time.

Register 2.7: BTBI_SLAVE_STATUS - RO (0x0000006) Status of the BTBI communication module when configured as slave.

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31 12	11 4	3 2 1 0
-	0x0	0 0 0 0 Reset

\mathbf{busy}	Busy receiving command.
wait_for_lock	Waiting for the ALPIDE Control module to lock.
err	ALPIDE Control didnt lock, or something wrong with RX.
armed	Slave is ready to receive trigger to execute command.
\mathbf{msg}	The messaeg received.



Register 2.8: BTBI_SLAVE_CMD - RO (0x00000007) The last received command to be executed if armed and triggered.

Register 2.9: NUM_TRIGGERS - RW (0x0000008)

The number of triggers to be transmitted of sequence commands. Valid for trigger, pulse and pulse/trigger commands.

31 0	
0x1	Reset

Register 2.10: TRIGGER_TO_EXECUTION_DELAY - RW (0x0000009)

Delay added between the transmission of trigger signal from master to slave, to the execution of commands on the master side. Minimum 7. Added to synchronize when the command is executed on all pRUs.

31	0	
0:	x7	Reset

Register 2.11: SLAVE_TRIGGER_TO_EXECUTION_DELAY - RW (0x0000000A) Delay added between the receiving trigger signal and the execution of the command on the slave pRUs. Minimum 2. Added to synchronize when the command is executed on all pRUs. Only change if one needs

to synchronize between slaves. 31 0 0x2Reset Register 2.12: SEQUENCE_DELAY - RW (0x000000B) For sequences: The number of clock cycles (40 MHz) between the execution of each command. Minimum 40 (time required to complete operation). 31 0 0x28Reset Register 2.13: PULSE_TRIGGER_DELAY - RW (0x000000C) Special delay for pulse/trigger sequence: delay between the pulse and the trigger command. Minimum 40 (time required to complete operation). 31 0 0x28Reset Register 2.14: NUM_TRAINS - RW (0x000000D) Specific for the trigger sequence: the number of trains to be transmitted. Trains are grouping of a number of triggers to be executed. 31 0 0x1Reset Register 2.15: TRAINS_DELAY - RW (0x000000E) The delay between each train - from train stop to it begins again - in 40 MHz clock cycles. Minimum 40 (time required to complete operation). 31 0 0x28Reset $\label{eq:register2.16: TRIGGER_SOURCE - RW (0x0000000F)} \end{tabular} Optional, used for data tagging. The source of the ALPIDE trigger signal. 0x0 = ALPIDE Internal Strobe$ Sequencer, 0x1 = External pRU Hardware Signal, 0x2 = Software trigger. Used in data tagging, 0x3 =FPGA Trigger Manager. Unused 31 1 0 0x3Reset $\label{eq:register} \begin{array}{c} {\rm Register \ 2.17: \ ALPIDE_MODE \ - \ RW \ (0x00000010)} \\ {\rm Optional, \ used \ for \ data \ tagging. \ The \ readout \ mode \ the \ ALPIDEs \ are \ configured \ in. \ 0x0 = TRIGGERED \end{array}$ mode. 0x1 = CONTINUOUS mode. Used in data tagging.

31

1 0

1 Reset

6



31	U	
	0x0	Reset